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Ripple-Free Flyback Converter with Passive Pulsating Ripple Cancelling Circuit

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Abstract

In order to solve the problems caused by the pulsating current ripple of switching-mode power converters, a passive pulsating ripple cancelling circuit (PPRCC) is proposed in this paper. The features of the proposed PPRCC include simple, modular structure, and high degree of design flexibility. By integrating the proposed PPRCC, an input current ripple-free flyback-type converter is adopted and analyzed as an example because of its comprehensive utilization in small power rating commercial products. In addition, the switch voltage spike offlyback converter can be suppressed by integrating the proposed PPRCC without using snubbers, it turns out the efficiency can be further improved. The corresponding operating principle, steady-state analysis, and zero ripple design criteria of the proposed PPRCC are provided. Experimental results show that the resulting peak-to-peak input current ripple is reduced and improved the efficiency can be achieved.

Keyword- Ripple-Free Flyback Converter, Passive Pulsating Ripple Cancelling Circuit (PPRCC)

I. INTRODUCTION

Current scenario a switching-mode power converter has become one of the key components in many widely developed systems such as distributed energy resource systems (DERs), electric vehicles (EVs), clouding servers, and various other applications because of its high efficiency and high power density features. However, several well-known problems of power converters such as electromagnetic interference (EMI), input/output power quality degradation, lower transient response, reduction on energy conversion efficiency, and shortening the lifespan of input sources are caused by the inherent current ripple. The simplest way to solve the problem caused by the current ripple is to use a bulky electrolytic capacitor a ripple filter. Nevertheless, it is well-known that electrolytic capacitors will reduce the lifespan of power converters. Another option is to integrate a LC filter with the power converters, however, LC filter causes efficiency degradation because of its series-connection with power converters. Therefore, several ripple cancelling techniques without using electrolytic capacitors and LC filters have been proposed in literatures for continuous current ripple reduction, several literatures have been proposed for providing ripple cancelling techniques, couple inductor or ripple filter is sued for eliminating current ripple. However, due to the integrated magnetic components, the current ripple reduction effect is sensitive to the coupling coefficient. Another comprehensively used technique is the interleaving control. According to the basic interleaving control algorithm, at least two-phase power circuits controlled by two180 degree shifted signals are needed in a power circuit. One of the advantages of the interleaving control is the input current ripple can be reduced. Nevertheless, focused on ripple cancelling effect, the interleaving control still suffers from several limitations. Such as it cannot be used in single-phase converter, more complex control scheme, and the ripple cancelling capability is dependent on the duty ratio of active switches.

For pulsating current ripple reduction, most of the techniques presented in recent literatures also use interleaving controls to achieve current ripple reduction. These papers focused on flyback-type power converters because of its simplicity and comprehensive utilization in small power rating commercial products. However, the limitations are then input current ripple cannot be completely cancelled, the interleaving control cannot be implemented in a single-phase converter, and extra active switches and control circuits are needed. Another pulsating current ripple reduction method used in single-phase converter is to integrate couple inductor into flyback converters. Nevertheless, the coupling coefficient of magnetic component has to be precisely designed during circuit implementation, otherwise the input current ripple-free cannot be achieved. It will cause the difficulties on power converter manufacturing. To overcome these problems, a passive pulsating current ripple cancelling circuit (PPRCC) is proposed this paper. The features of the proposed PPRCC include: (1) the ripple cancelling effect is not impacted by coupling coefficient, (2) it is easy to be integrated into single phase power converters with simple design criteria, (3) only small ripple power needs to be processed so that the efficiency of converter will not be much degraded and the size of the circuit can also be reduced.

II. PROPOSED SYSTEM

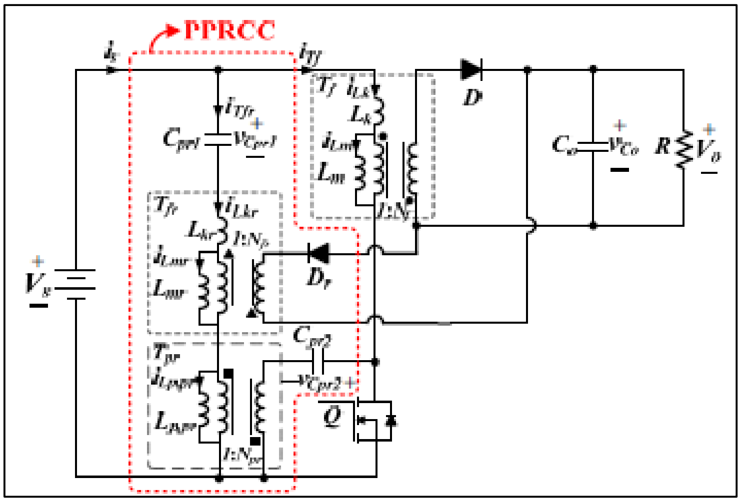

Fig. 1: proposed input current ripple-free flyback-type converter

The circuit configuration of the proposed current ripple-free flyback-type converter are shown in Figs. 1, respectively. one can see that the proposed PPRCC is integrated into the input side of a -+conventional flyback converter to eliminate the input current ripple. It turns out that the input current of the proposed converter can be a pure DC current. The proposed PPRCC consists of a ripple mirror transformer Tfr, a high frequency transformer Tpr, a ripple delivery diode Dr, and two blocking capacitors Cpr1 and Cpr2.

The ripple mirror transformer Tfris operated as a flyback transformer and is used to mirror the original pulsating ripple current flowing into the flyback transformer Tf. Like the original flyback transformer Tf, the ripple mirror transformer Tfris modeled as an ideal transformer with turns ratio Nfr, a leakage inductor Lkr, and a magnetizing inductor Lmr. On the other hand, the high frequency transformer Tpris used to induce a voltage from the secondary side to the primary side so that an expected voltage can be constructed across the magnetizing inductor Lmrduring each operation mode of the proposed converter. For simplicity, Tpris modeled as an ideal transformer with turn's ratio Nprand a magnetizing inductor Lp, pr but without including an equivalent leakage inductor. In addition, the blocking capacitors Cpr1 and Cpr2 are used to block the DC power from the input source so that only very small power needs to be processed in the proposed PPRCC.

A. Modes of Operation

Mode 1 - Switch Q is turned on. Diodes D and Drare reverse-biased. The corresponding equivalent circuit is shown in Fig. 4(a). The magnetizing inductor Lm and the leakage inductor Lkare charged by the input voltage source Vsso that iLm(=iLk) is linearly increased, which is also equal to the current iTf flowing into flyback transformer Tf. On the other hand, the capacitor voltage vCpr2 is reflected to the primary winding of Tpr, and the voltage across the leakage inductor Lkrand the magnetizing inductor Lmrwill be a negative value (vLkr+vLmr=Vs－vCpr1－(1/Npr)vCpr2). Therefore, the current iLmr(=iLkr) is linearly decreased, which is also equal to the current iTfrflowing into ripple mirror transformer Tfr. Hence, iTfrcan be used to compensate the ripple of iTf. Meanwhile, the output power is supplied from the output capacitor Co.

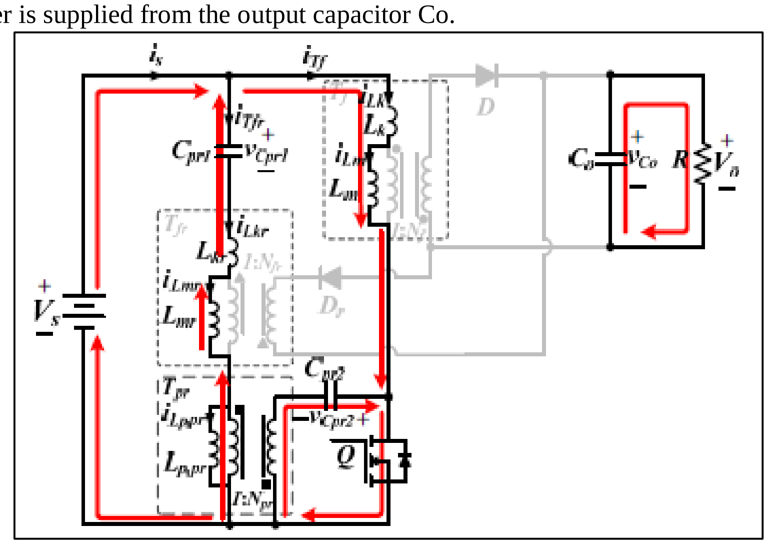

Fig. 2: Mode 1

Mode 2 - Switch Q is turned off. Diodes D and Drare forward-biased. The corresponding equivalent circuit is shown in Fig. 4(b).The voltage across the magnetizing inductor Lm is a negative value (vLm= (1/Nf)Vo) so that the current iLm is linearly decreased. The energy stored in Lm is now released to the output of converter through the diode D as usual. On the other hand, the voltage across the magnetizing inductor Lmr is a positive value (vLmr=(1/Nfr)Vo) so that current iLmr is linearly increased. The energy stored in Lmr is now also released to the output of converter through the ripple delivery diode Dr. In this mode, the current iTf flowing into flyback transformer Tfisequal to the leakage inductor current iLk, and the current iTfrflowing into ripple mirror transformer Tfris equal to the leakage inductor current iLkr. Like Mode I, iTfr can be used to compensate the ripple component of iTf. It is worth mentioning that, observing Fig.3 and comparing it with the conventional flyback converter, one can see that when switch is turned off, the current iLk continuously flows into capacitor Cpr2. Hence, the energy stored in the leakage inductor Lk can be released to the capacitor Cpr2. In addition, the voltage across the switch will be clamped by the sum of capacitor voltage vCpr2 and the secondary-side voltage of Tpr. It helps to reduce the turn-off voltage spike across the main switch so that the conversion efficiency of the proposed converter can be further improved.

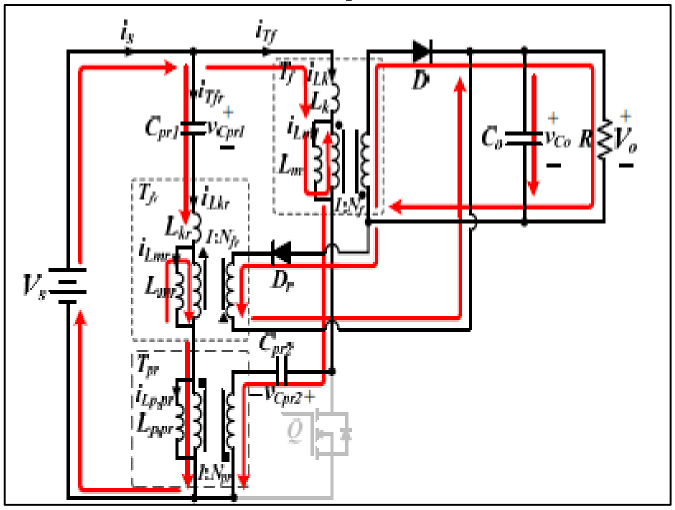

Fig. 3: Mode 2

In the following, voltage gain, average capacitor voltage, ripple-free design criteria, and blocking capacitor voltage ripples of the proposed converter will be derived. The voltage gain of the newly-constructed input current ripple-free flyback-type converter will not be affected by integrating the proposed PPRCC. Because leakage inductance usually is much smaller than magnetizing inductance, for simplicity, the voltage across leakage inductance is neglected for deriving the average capacitor voltage. In order to achieve zero input current ripple, the current slope of input current dis/dt should be zero so that can be obtained. Once the variation in capacitor voltage vC from its average value VC is negligibly small (i.e., voltage ripple is very small, vC=VC), the capacitor voltage can be assumed as a constant voltage. One can see that can see that the voltages across Cpr1 and Cpr2 are used to\ construct a constant voltage on the primary side of the ripple cancelling transformer Tfr in each operation mode. Then, the voltage on the primary side of Tfr will be an additive inverse of the original flyback transformer Tfin each operation mode. It turns out the slope of the current iTfr can be used to compensate the slope of the current iTf. Hence, the voltage ripples ΔvCpr1 and ΔvCpr2 which across Cpr1 and Cpr2 may further influence the ripple cancelling effect so that it should be minimized for achieving well ripple reduction.

In order to make a fair comparison, a RCD snubber is used in the conventional flyback converter so that the low-voltage rating MOSFET same as used in the proposed converter can also be used. The efficiency curves of the proposed converter and the conventional flyback converter using low-voltage rating MOSFET are represented as the blue and purple lines in respectively. One can see that once a lower voltage rating MOSFET is used for the proposed converter, the efficiency of and 100W load conditions can be achieved, respectively. As compared with the conventional flyback converter with snubber, approximately improvement in efficiency at and load conditions can also be achieved, respectively. It is worth mentioning that for the conventional flyback converter, the energy of voltage spike is dissipated on the snubber resistor. For the proposed converter, the energy of voltage spike is first released to the capacitor *Cpr2* then it can be delivered to the output load. Therefore, the power consumption of the proposed PPRCC is smaller than a conventional snubber circuit at heavy load condition.

III. CONCLUSION

In this paper, a simple and modular structure PPRCC is proposed to eliminate the input pulsating current ripple of the conventional flyback converter effectively. It turns out that the input current of the newly-constructed current ripple-free flyback-type converter can now be a nearly pure DC current. Experimental results show that the peak-to-peak pulsating current ripple of a conventional flyback converter can be eliminated by the proposed PPRCC, which corresponds to a ripple reduction effect. Furthermore, by integrating the proposed PPRCC into a conventional flyback converter, the power switch can be replaced with a lower voltage rating device. According to the experimental results, comparing with the conventional flyback converter, it can be seen that improvement in efficiency can be achieved at load condition.

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