Design and Analysis of Different Circuits using DCVSL & Static CMOS Technique

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Abstract

The basic requirement of any Integrated Circuit is high speed and low power processing of the data signals to perform the desired execution. The minimization of feature size plays an important role in increasing the performance of integrated circuits. However, the minimization of ICs has affect on leakage current when compared to the total current requirement of the circuit. So in this work presents the design of single bit magnitude comparator & 3 input EXOR gate using conventional CMOS logic style as well as DCVSL style. Then, the comparison has been carried out for both the designs with some parameters. These parameters are power dissipation, delay and how much transistors have been used in the respective designs, and then concluded that which design yields best results accordingly. In CMOS circuits, as the technology scales down to nano scale, the sub-threshold leakage current increases with the decrease in the threshold voltage. So we need a technique to tackle the power dissipation problem in CMOS circuits do the analysis keeping parameters such as power consumption, delay, voltage & transistor count. First, there is the analysis between power consumption & delay, keeping the voltage constant at 5V. We here can see that circuit of the DCSVL structures produces better results in terms of power consumption by lowering its value. The circuit designed using DCVS Logic style is an attempt to further reduce the power dissipation with minimum delay.

Keywords- CMOS, DCVSL, Magnitude Comparator, EXOR Gate, VLSI, Tanner EDA

I. INTRODUCTION

The semiconductor industry in now - a- days are downsizing as per the Moore‘s law of scaling. Scaling has directly or indirectly been the root cause of the tremendous capabilities of today‘s ICs and their ubiquitous use in nearly all modern electronic systems [1]. In order to perform the desired execution by any IC (Integrated Circuit), is the basic requirement for any logic. The minimization of feature size plays an important role in increasing the performance of integrated circuits. But the feature minimization inversely affects the percentage of leakage current when compared to the total current requirement of the circuit [5]. The increasing prominence of portable systems and need to limit the power consumption in very high density VLSI chips results in rapid and innovative growth of low power design. In several high performance designs, the leakage power consumption is becoming comparable to that of switching component [8]. High power consumption leads to reduction in battery life in case of battery powered applications & also affects the reliability and cooling cost. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. [2] The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. Thus the aim of low power design for battery powered devices is to enhance the service life of battery while fulfilling the performance requirements. There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating and drowsy method. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But power supply voltage scaling results in reduced noise margin. Forward body biasing methods and dual threshold techniques are used to reduce sub threshold leakage current.

II. DESIGN IMPLEMENTATION

With concerned to tackle the power dissipation problem in CMOS circuits, the analysis performed on the parameters such as power consumption, delay, voltage & transistor constant. In this work one can easily observe that circuit of the DCSVL structures produces better results in terms of power consumption by lowering its value than CMOS logic style [10]. The circuit designed using DCVS Logic style is an attempt to further reduce the power dissipation with minimum delay. Now a days, the concern is for low power, high speed and minimum area for designing the circuit [8] [9]. For that intensified research is going on low power, high speed of operation of the embedded system. The digital magnitude comparator is the elementary component in the digital system which is used for performing arithmetic and logical operations. Research is going on for increasing speed and complexity of a large scale integrated system. When technology is scaled down, execution of device enhances however it has got to be distinctly essential for any device to be power efficient.

In order to reduce the complexity and circuit delay for implementation of complex Boolean logic, the differential pairs of MOSFET devices are cascoded. The digital logic networks with N-high cascoding of differential pairs of NMOS devices are capable of processing Boolean functions with up to (2N-1) input variables [7]. Thus, this provides an advantages in performance up to four times when compared to standard CMOS NAND/NOR logic families. The primitive NAND/NOR Logic and the DCVSL, both are potentially dense and are well-suited with previous design automation tools [6]. Using cascoded high-performance NMOS devices, logic trees which are compatible in nature are designed and the unstacked P mosfet devices are used as pull-up devices in load and buffer circuitry [7]. Thus, the P-MOS devices can be optimized and hence critical spacing between P and N devices is relaxed. This reduces the device complexity for DCVSL designs. However, CMOS is widely used in for designing of logic circuits, but then also the DCVSL has its own features such as no static power, higher speed as it produces complementary outputs due to dual rail logic and is very efficient in designing any logic circuits. In VLSI, the delay modeling is calculated by value of capacitance for rising and falling transistors is obtained with uniform gate capacitance and diffusion capacitance rate/unit width with assumption of uniform P to N size ratio for various logic gates.

A. Logic Design using Conventional CMOS

In VLSI, the CMOS technology is one of the most popular and common technology which is broadly used to fabricate integrated circuits for numerous applications. This is the first technology that uses both P channel and N channel semiconductor devices together. Figure 1 represents circuit of CMOS Inverter. It consists of a NMOS & a PMOS transistor. If input at logic low then both of the gates are at zero potential & PMOS is ON that provide low impedance path from supply voltage to output. Therefore output approaches to high level of VDD. If input is at logic high then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output. Therefore, output approaches to the low level i.e. 0V.

CMOS logic style is really the extension of CMOS inverters to multiple inputs. Logic network of CMOS style is shown in Fig.1 (b). The principle of CMOS logic design says that Pull up network has only PMOS circuit& Pull down network has only NMOS circuit. The function of PUN is to provide a connection between output & VDD, similarly of PDN is to provide a connection between output & GND. The number of transistors for the N-input logic gate is 2N. Each logic stage contains pull up and pull down networks controlled by input signals. The pull up network contains p channel transistors. The pull down network is made of n channel transistors. If the pull up network is 'on', the pull down network is 'off' and vice versa. Thus, PUNs & PDNs never turns on together hence there is no static power consumption. The most common design style in modern VLSI design is the Static CMOS logic style [10]. The pull up network contains p channel transistors, whereas the pull down network is made of n channel transistors.

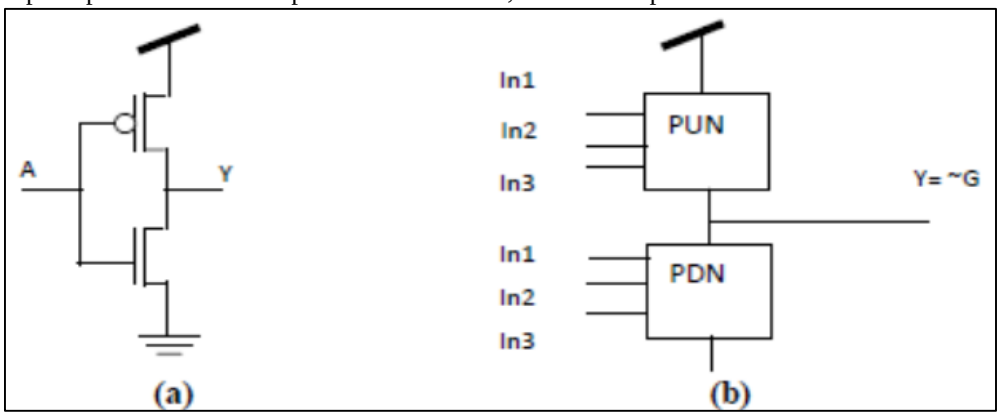


Fig. 1: (a) Circuit of CMOS Inverter, (b) Logic Network of CMOS Style

The major Advantages of this design style are that it provides full output voltage swing between 0 and VDD. Hence also provides high noise immunity because it is less sensitive to noise, and Provides high noise margin because VOH& VOL are approximately VDD & GND respectively. The conventional CMOS logic style has very low static power dissipation, High noise margins (full rail to rail swing), low output impedance, high input impedance, no steady state path between VDD and GND.

While on the other hand this style produces large Power dissipation. Also circuit implementation using conventional CMOS logic style requires a large number of transistors because for every input both (NMOS & PMOS) are used.

B. Differential Cascode Voltage Switch Logic

As the ICs are easily finds in any consumer electronics, Communications and high speed computing devices, the need of power efficient VLSI & system design is required. Thus the advancement in CMOS technology, there is a new interest in reducing the power with increasing chip density and operating frequency along with corresponding decreasing feature size. The one can easily find that in portable systems there is excessive power dissipation, due to this, the chip life shortens due to overheating with degrading performance. Portable systems with low power consumption has directed to advanced developments in Low Power VLSI design in recent years. The driving forces that are essential for portable devices are low power consumption and high throughput due to their increased complexity, small chip area, large density of components and high frequencies. A DCVS Logic is based on 2:1 Multiplexer which is used as an important element in many various circuit designs such as implementation of memory circuits and FPGA [11]. It is valuable in situations where price is a factor and for modularity [12].

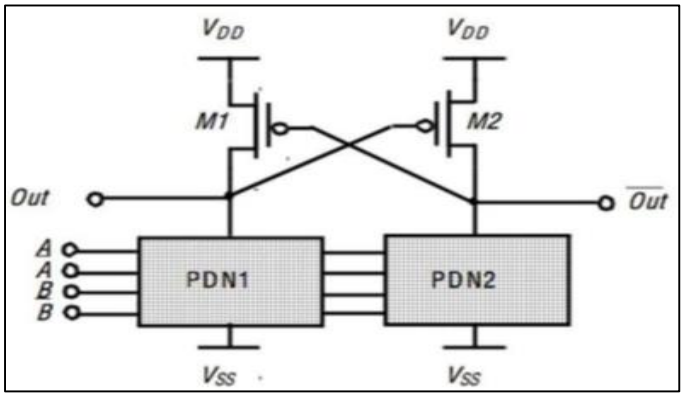


Fig. 2: Schematic of DCVSL logic style

According to the figure 2, the nodes out and ~Out are either pulled high or low according to the switching of the inputs. The DCVSL is designed differentially for the given logic in which the true and complementary inputs to the gate produces the complementary outputs [8]. This structure also consumes no static power, like standard CMOS, and also it utilizes the latches in order to generate the output. In this logic style, large PFETS are eliminated from each logic function, which allows complex circuits to consume low power. A logic function and complement of it is inevitably realized at the same stage [8][9]. This style can be divided into two basic parts a differential latching circuit and a cascaded complementary logic array [16]. DCVSL is a differential method which requires both true and complementary signals to be routed to gates. Two complementary nMOSFET switching trees are constructed to a pair of cross-coupled pMOSFET transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding nMOSFET network [10]. The differential output is then latched by the cross-coupled pMOSFET transistors. Since the inputs drive only the nMOSFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic. The advantage of DCVSL is in its logic density that is achieved by elimination of large pMOSFETs from each logic function. Both pull down networks in the Fig. 2 will never conduct at the same time [5].

III. CIRCUIT ANALYSIS

This section shows the circuit analysis for Magnitude Comparator and 3-Input XOR gate by basic CMOS style and DCVS logic style. The complete analysis has been conducted by the Tanner EDA. With 180nm, 65nm and 45nm technology for constant voltage of 5V.

A. Magnitude Comparator

A magnitude comparator is a combinational circuit that compares two numbers, A and B, and then determines their relative magnitudes. A > B, A = B, A < B. To determine if A is greater than or less than B, we inspect the relative magnitudes of significant digits. If the two digits are equal, we compare the next lower significant pair of digits. The comparison continues until a pair of unequal digits is reached. A magnitude comparator is a combinational circuit that compares two numbers A & B to determine whether: A > B, or A = B, or A < B. Input A is n-bit number & Second n-bit number B, Outputs will be three: output signals (GT, EQ, and LT), where: 1. GT = 1 IFF A > B, 2. EQ = 1 IFF A = B, 3. LT = 1 IFF A < B.
*Note: Exactly One of these 3 outputs equals 1, while the other 2 outputs are 0`s.

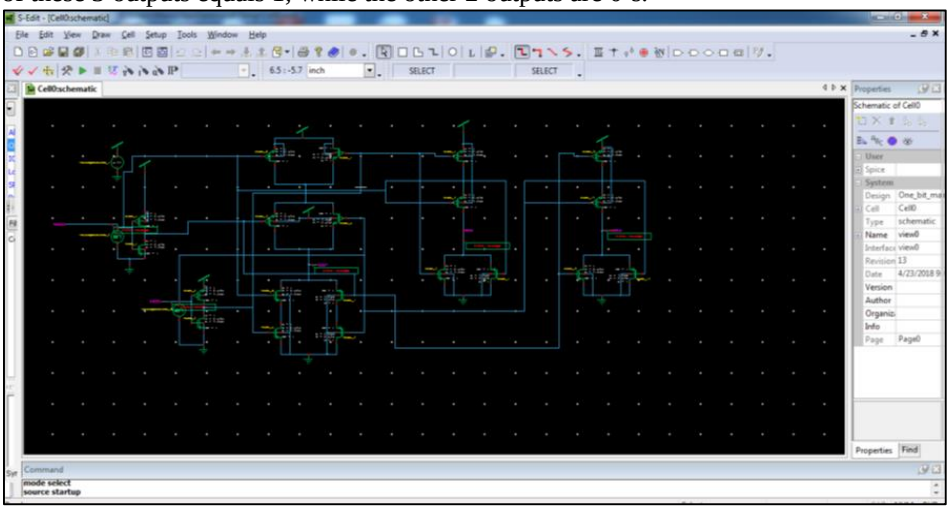


Fig. 3: Single bit comparator using CMOS logic style

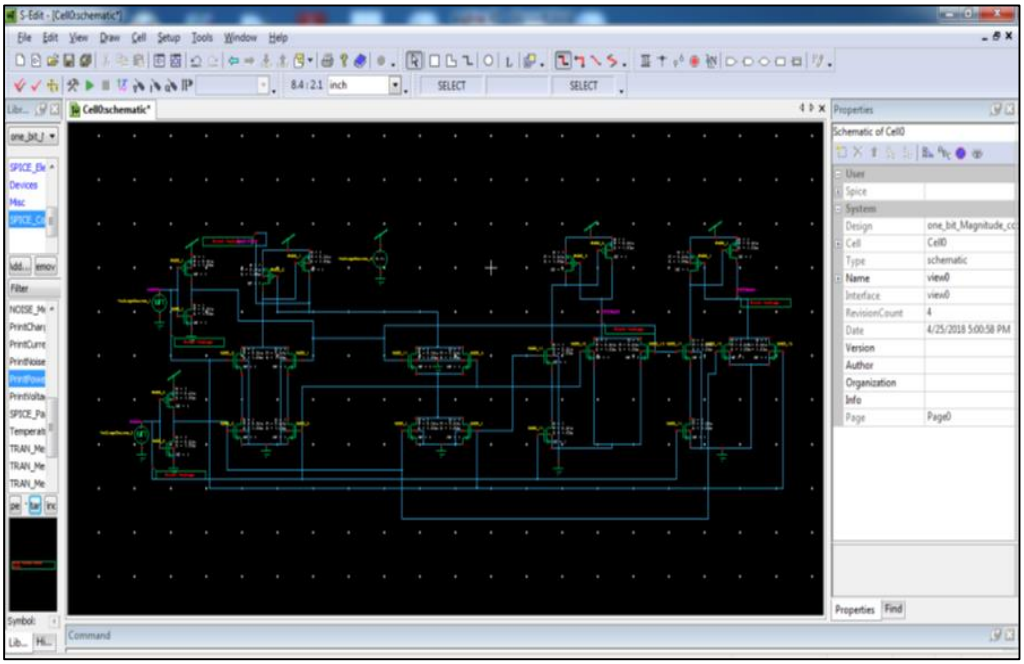


Fig. 4: Single bit comparator using DCVS

In this style the transistor count goes up to 8 PMOS and 18 NMOS. The 18 NMOS's body are connected to the source of the NMOS and the source of the NMOS is connected to the ground and is internally connected to other NMOS's source. For PMOS, the body and the source are connected to VDD. The simulated waveform for the circuit designed by varying both the inputs accordingly with magnitude as 5.0v is shown in figure 4. Consider input bits as 10 then referring to truth table in the output side, 1 should be obtained in A>B & rest of the output will be obtained as 0. After performing simulation the output waveform (Fig 5) shows the same result as in truth table for the applied input bits.

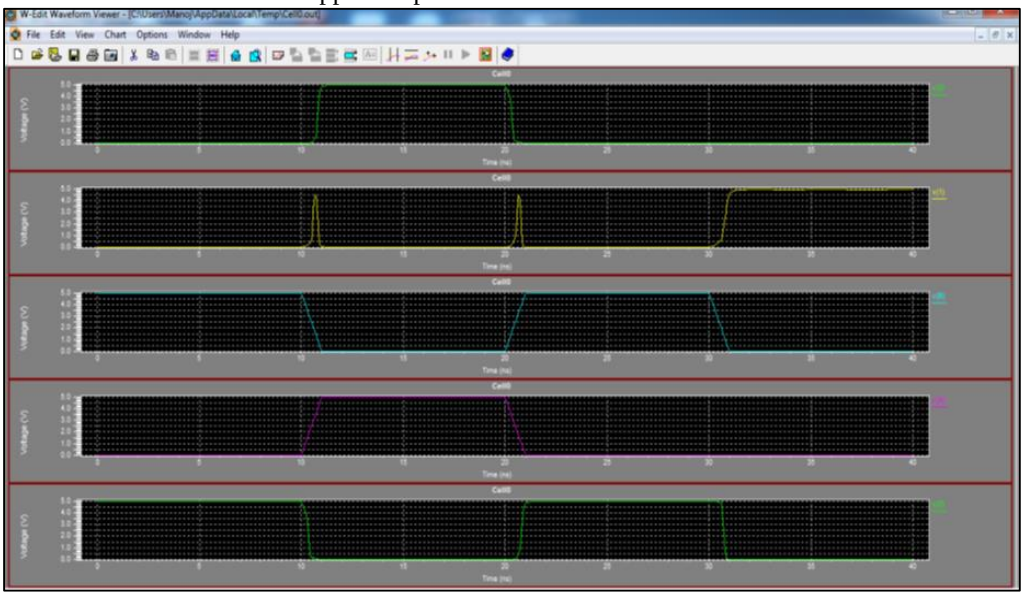


Fig. 5: Output waveform of magnitude comparators

B. XOR Gate (3-Inputs)

EXOR Gate is most used gate after NAND gate and nor gate and is directly used in other circuits. Main uses of EXOR Gate are in parity checking e.g. let a system is receiving a continuous stream of data in some fixed packet size. The parity checker can help to know whether the data received is correctly or not.

And the other use in very fundamental circuit used widely across digital design i.e. Adder (Half). The XOR gives the sum of two 1 bit numbers. EXOR Gate can also be designed using other gates. For designing a EXOR gate only 4 NAND gates are required also if we want to design EXOR gate using NOR gates only then only 5 gates are required to yield an EXOR gate.

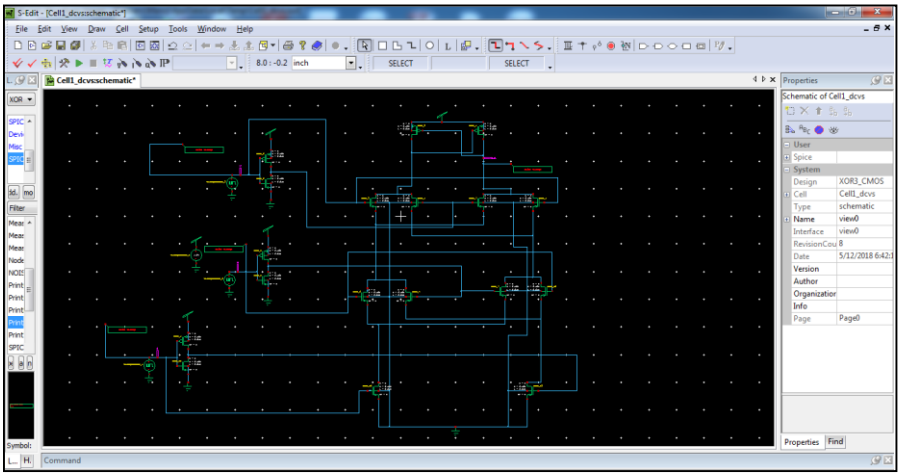


Fig. 6: 3 - Input XOR gate using CMOS

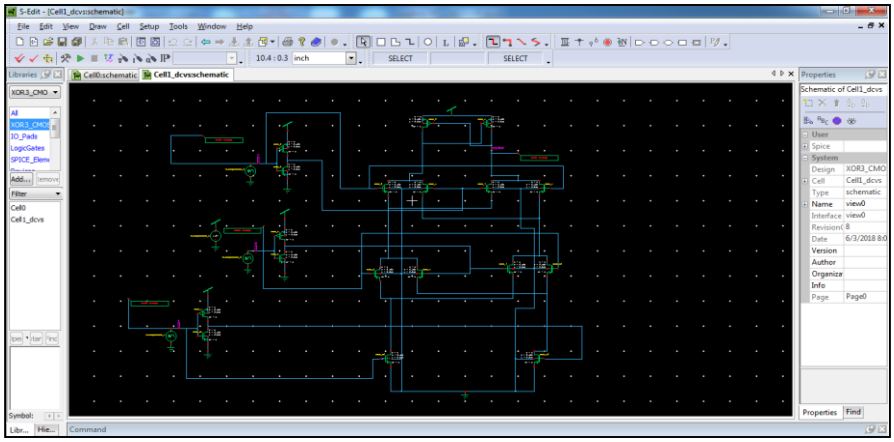


Fig. 7: 3 - Input XOR gate using DCVS

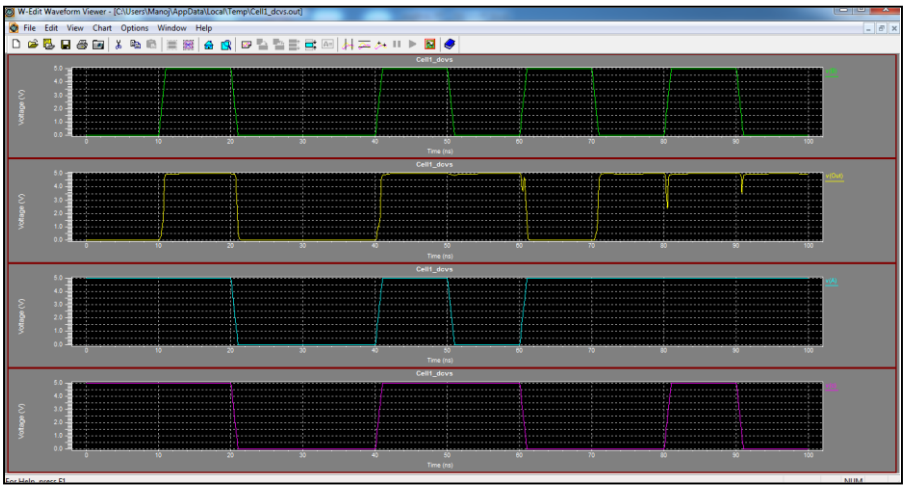


Fig. 8: Waveform output for 3-Input XOR gate

XOR Gate also has some other interesting uses:

Very useful application of EXOR gate is a controlled inverter .When one of the inputs is used as a control and other as data input. If the control = 1 then the output is the inverted version of input. If control = 0, then output = input. So, the control bit can be used to implement two's complement arithmetic in hardware.

One of the most important uses is that it makes up a part of a half-adder circuit, which is a fundamental building block of the CPU inside a computer. Any number XOR itself is zero. This is sometimes used in machine code to clear a register. If you XOR by the same number twice, you get the original value back. And, of course, you can use it any time your program logic is "one or the other, but not both.

XOR is useful to find degree of correlation between two strings as it produces a 0 when both inputs match.

An XOR gate is used for figuring out whether the number of input bits is odd (00 and 11 are even, 01 and 10 are odd). It literally means "exclusive or," in the sense of "one or the other, but not both."

Both EXOR Gate and single bit magnitude comparator is designed using DCVSL & CMOS logic style and then they are compared on behalf of some parameters. These parameters are Power Dissipation, Delay & Transistor count.

IV. CONCLUSION

For low-leakage and high-speed circuit, the important two factors are speed and power. However, the main trade-off is that; when someone goes for speed, the power is degraded. And in the next case, when the power consumption is improved, the delay is more in that case. Therefore, we go for the power delay product, which best determines the efficient circuit combining the two parameters, keeping other factors such as voltage and transistor count. Also find a technique which results in reduction of both power dissipation and delay, also number of transistors used while designing the circuit. When the power consumption is considered, we find out that the DCVSL structures produces better result in case of the both circuits than the conventional one and the best among them being the Static DCVSL; whereas when the delay is measured the DCVSL alone produces better result in case of the both circuits than the conventional one. Now, considering the power delay product for these three structures, we find out that the PDP is less for the EXOR & magnitude comparator circuits in case of the Static DCVSL, whereas for conventional CMOS logic style circuit, it is more. Coming to the DCVSL EXOR circuits which are implemented using the static DCVSL structures, we find out that the power consumption is less in case of the circuit.

Table 1: Number of Transistors for various Design

S.No.	*Circuit*	*Technology*	*Number of Transistors*
1.	*Magnitude Comparator*	*CMOS*	*24 [12P+12n]*
		DCVS	*26[8P+18N]*
2.	*3-XOR*	*CMOS*	*32[16P+16N]*
		DCVS	*18[3P+15N]*

As this is an EXOR gate circuit, therefore it has one output, i.e. out. So, for delay, it is calculated separately.

And from the analysis, we find out that the delay for this circuit is lesser than the circuit which is designed using conventional CMOS method. For power dissipation the values are more for conventional CMOS structures.

Table 2: Power Dissipation for Comparator with different technology scale (mW)

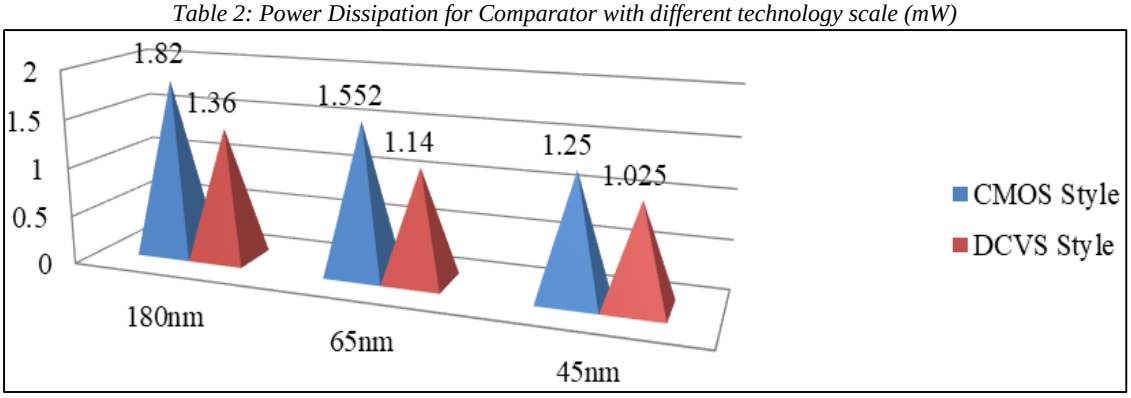
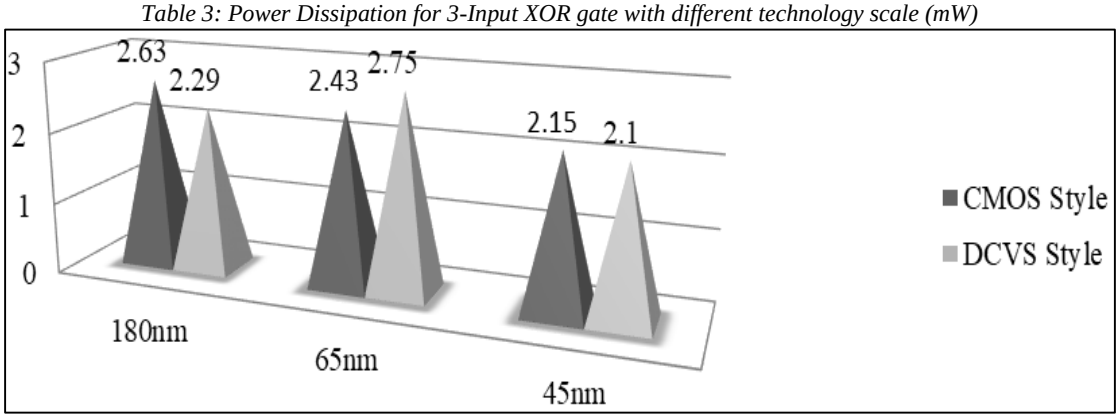


Table 3: Power Dissipation for 3-Input XOR gate with different technology scale (mW)



In calculation of the Power Delay Product (PDP) for all of these EXOR & magnitude comparator circuits, it is found out that the proposed circuits of all of them are having less value than the conventional one and static DCVSL adder is having the least among them. An analysis is done with the parameters number of transistors, which shows that the area is least for the static DCVSL

comparator than the rest and the number of transistors is least for the Static DCVSL than the conventional CMOS. So considering all the scenarios, according to the results obtained Delay, Power dissipation &number of Transistors used in the circuit is lesser for the circuits.

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