Power Gating Techniques For Nano-Scale Devices

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Abstract

Power consumption is one of the major issues in CMOS technology. ITRS reports that leakage power may dominate the total power consumption. As technology feature size shrinks, the static power dominates the dynamic power consumption. This is known as the sub-threshold leakage which rises by creating a weak inversion channel between drain and source. Gate oxide thickness reduces as technology decreases which increases the sub-threshold leakage. Along with sub-threshold leakage there is an increase in ground bounce noise. This paper reviews different stacking techniques proposed in other papers. But each of those papers had certain trade-offs. So, a combination of the existing techniques has been implemented to have minimal sub-threshold leakage, ground bounce noise and propagation delay.

Keywords- CMOS Nanoscale, Subthreshold Leakage, Stacking Transistors, Ground Bounce Noise

I. INTRODUCTION

Power consumption in nanoscale based CMOS circuits is mainly categorized into two types. Semiconductor nanomaterials such as quantum dots, nanowires, or nanobelts have attracted tremendous attention due to their unique properties of electronic and optical as compared to their bulk properties which has led to scaling down of the size of the transistors used in CMOS circuits [1-5]. One of the main concerns in these nanoscale based CMOS devices is the dynamic power consumption and the other is static power consumption. Dynamic power consumption is also known as switching power consumption which is dissipated mainly when the nanoscale based transistor is in working mode. Static power is also called the sub-threshold leakage. For 180nm technology static power contributes only 10% of the total power. But as technology size shrinks it becomes comparable to or even greater than dynamic power. Other side effects of this feature shrinkage is the decrease of supply voltage and threshold voltage. As the threshold voltage decreases, sub-threshold voltage increases which affects the battery life of the technology. One possible temporary solution is reducing the supply voltage. The most efficient way to reduce this leakage is to use power gating schemes that use large transistors called "sleep-transistors" in series with pull-up and pull-down transistors to cut off the circuit from power supply when it is in standby mode. Along with the increase of sub-threshold leakage, ground bounce increases too. Ground bounce also known as simultaneous switching noise defines a condition when a device's output switches from High to Low and causes a voltage change on other pins. Ground bounce is an inductive noise associated with clock gating. Different variations of the stacking techniques are discussed which help reduce the sub-threshold leakage and also the ground bounce noise.

Section II discusses some of the previous approaches. Section III discusses the results and trade-off of the techniques discussed. Section IV discusses a possible new technique based on the combination of the previous techniques and its results. Section V discusses the final conclusion.

II. ANALYSED INNOVATIVE STACKING TECHNIQUES

All the techniques described here are based on the stack effect, this is because when there are two or more stacked off-transistors (as shown in the following figure), and the sub-threshold leakage is reduced. This is because, turning OFF more than one transistor in a stack of transistors forces the intermediate node voltage to go to a value higher than zero. This causes a negative Vgs, negative Vbs (more body effect) and Vds reduction (less DIBL) in the top transistor, thereby reducing the sub-threshold leakage current flowing through the stack considerably. It also increases the circuit density and decreases the wre length.

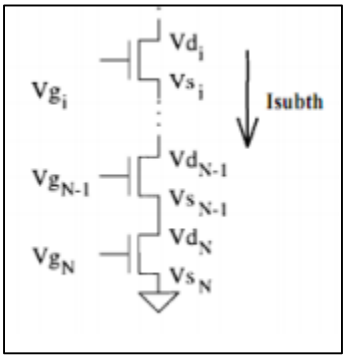

Fig. 1.0: Stacked transistors

Leakage is categorized into two different factors:

- State Saving Technique: It preserves the logic state in both active and sleep mode.
- State Destructive Technique: It preserves the state in active mode but loses the state in sleep mode.

The different approaches are listed below:

A. Sleepy Stack Approach

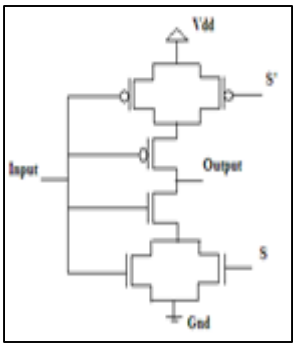

Fig. 1.1: Sleepy Stack Approach

In this method two transistors are stacked with the inverter circuit and two sleep transistors are parallel with the inverter circuit in both pull-up and pull-down network. This approach works in two modes, in active mode when S=1, S'=0, two sleep transistors are ON and if input =0 the two PMOS transistors are ON in the pull-up network. So, there is high internal resistance in between the pull-up network which suppresses the leakage dramatically. But this approach has a trade-off which is area overhead and increased propagation delay.

B. Sleepy Keeper Approach

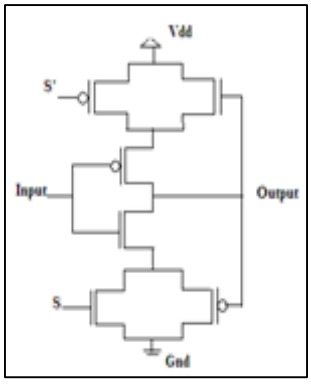

Fig. 1.2: Sleepy Keeper Approach

In this technique, two sleep transistors are parallel in both pull-up and pull-down network. These two extra sleep transistors are used to save the logic state. The leakage reduction is moderate in this method. During the sleep mode two extra transistors are turned ON to save the logic state. So this is obvious state saving technique.

C. Dual Sleep Method

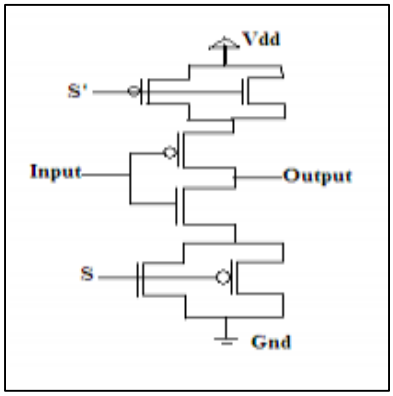

Fig. 1.3: Dual Sleep Method

In Dual sleep method, two sleep transistors are arranged similar to the sleepy keeper method. In both active and inactive mode two sleep transistors are always ON in both pull-up and pull-down network. So, output is always connected to gnd and Vdd. This is a state savings technique. This method has excellent trade-offs between power, delay and area.

D. Dual Threshold Transistor Stacking

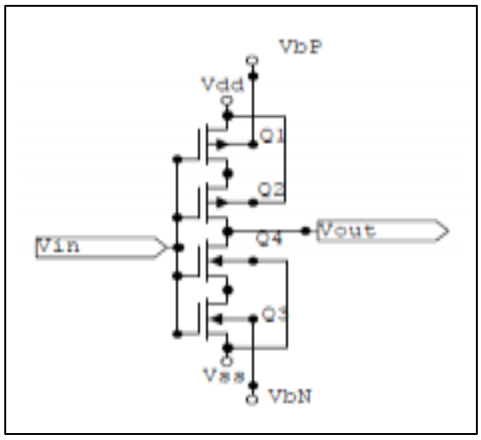

Fig. 1.4: Dual Threshold Transistor Stacking

In dual threshold transistor stacking technique the body of one transistor is connected with the other body of the other stacked transistors. So, when one transistor is ON the threshold of another body connected transistors is also changed. This reduces the sub-threshold leakage while maintaining the dual threshold voltage. The trade-off in this method is the propagation delay and area overhead.

E. Novel Common Vdd and Ground

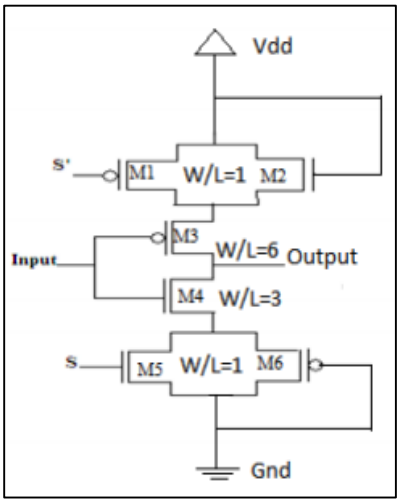

Fig. 1.5: Novel Common Vdd and Gnd

This technique is a variation of two prior techniques namely sleepy keeper approach and dual sleep method. In the block diagram, sleep transistors (M1 & M5) are parallel in both pull-up and pull-down network with two extra transistors (M2 & M6). The two extra transistors (M2 & M6) are used for saving state because in both active and sleep mode M2 and M6 transistors always have contact with output and ground. In this novel architecture, both pull-up and pull- down network have an aspect ratio of w/l=1 and aspect ratio w/l=6 and w/l=3 is maintained respectively in transistors M3 and M4. The main feature in this technique is that, M2 transistor is connected with the power rails and M6 transistor is connected with the Gnd. So, in active mode pull-up NMOS M2 transistor is always ON and Inactive mode pull-down PMOS M6 transistors is always ON. So, in both active and inactive mode output has an always connectivity with the Vdd and Gnd. During active mode, S=1 and S'=0, and all sleep transistors (M1 & M5) are turned ON. Due to the added sleep transistor, the resistance increases, and the propagation delay decreases leakages reduce.M1 and M3 transistors are ON so the internal resistance increases which reduces the leakage dramatically. This technique saves the state in both active and inactive mode so it is a state saving technique.

F. Stacking Power Gating Scheme

Strategy to reduce ground bounce noise is first to isolate the ground for a small duration during mode transition and to turn on the M2 transistor in linear region instead of saturation region to reduce the current surge. When transitioning from active to sleep mode M1 is turned on first and after a small delay M2 is turned on. During this short delay ground bounce is greatly reduced by controlling the intermediate node voltage which can be controlled by the proper selection of capacitance C.

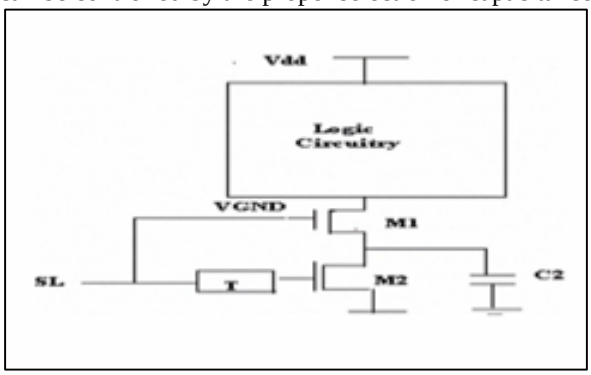

Fig. 1.6: Stacking Power Gating Scheme

Stacking power gating basically has three modes of operation i.e. active, standby and sleep to active mode transition.

In active mode, the sleep signal of the transistor is held at logic '1' and both the sleep transistors M I and M2 remain ON. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the circuitry approximately equal to the supply voltage. So,

Voltage across the capacitor CI =VCI (active mode) = V (RloN) + V (R2 ON) Voltage across capacitor C2 =VC2 (active mode) = V (R2ON) = OV.

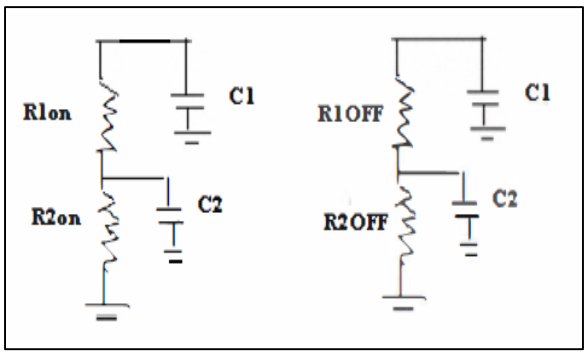

Fig. 1.7: Equivalent circuit of sleep transistors Ml and M2 in (a) active mode, (b) standby mode

To reduce the leakage current in the sleep mode, power supply rail and ground rail are isolated by turning OFF the sleep transistors. The sleep signal SL is held at logic '0' to switch OFF the sleep transistors M I and M2. R I OFF and R20FF are M I and M2 OFF resistances, and offers very high resistances. So there is no discharging path for CI and C2 transistors. The capacitor CI will charge up to the VDD. Capacitor C2 charges to small amount of voltage, because most of the charge is acquired by the capacitor C1, giving no path for capacitance C2 to charge. As high threshold voltage sleep transistor MI is OFF, it potentially blocks the leakage current to charge up the capacitance C2. In standby mode capacitance C1 (virtual ground node) has been charged up to V1 and the capacitor C2 has been charged to V2. So,

Vel (standby mode) = VI, VC2 (standby mode) = V2

In sleep to active mode transition, initially MI is turned ON. After a small delay transistor M2 is tuned ON to reduce the ground bounce noise. The voltage across capacitors C1 and C2 remain unchanged, at the event when MI transistor is ON. Here the resistance R20FF is high and M2 as an open switch. When LlT > t > 0, the circuit is a source free circuit. In this period the capacitor C2 will be charged.

G. Diode Based Stacking Power Gating Scheme

Incorporating a diode sensor as a sleep transistor in the power gating scheme is called diode based stacking power gating scheme is also challenging at a nanoscale based devices. Lot of research in the field of nanoscale sensors has been done to develop sensors to incorporate them as sleep transistors for its in these devices [6-9]. We can get more ground bounce noise reduction by incorporating this strategy. This is possible by

- Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of GBN.
- Isolating the ground for small duration during mode transition.
- Turning ON the S2 transistor in linear region instead of saturation region to decrease the current surge.

There are several benefits of combining stacked sleep transistors with capacitors. First the magnitude of power supply fluctuations/ ground bounce noise during mode transitions will reduce because these transitions are gradual. Second, while conventional power gating uses a high- threshold device as a sleep transistor to minimize leakage, a stacked sleep structures can achieve the same effect with a normal threshold device.

III. Results Of The Analysed Methods

The goal of the study done on various aspects of power gating while keeping several factors in check. On comparison of the various techniques on dynamic power consumption, we can see there is a huge improvement at higher nm scale, but at 32 nm architecture, we can see there is only a small reduction in dynamic power consumption.

We find a similar behavior in the propagation delay studies of various techniques. But there is a significant reduction of propagation delay as we go lower in size. Static power reduction when compared against sleepy stack and dual sleep approach is significant. But the gain in not noticeable when compared with sleepy stack.

Through these studies, we can see that the gains outweigh its shortcomings. This approach remains promising, but it doesn't solve a few problems like ground bounce noise which occur at a nano-meter scale.

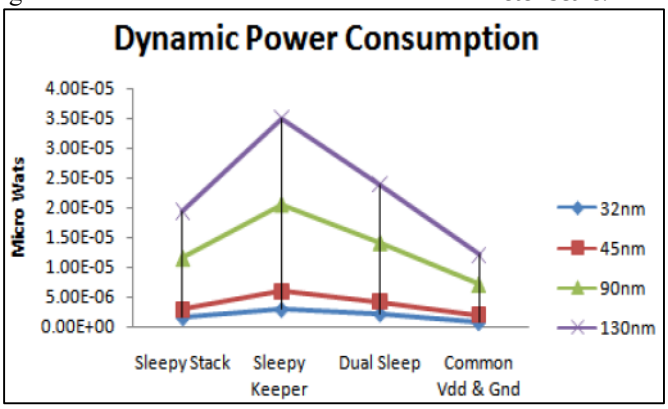

Fig. 2.0: Dynamic Power Consumption comparison

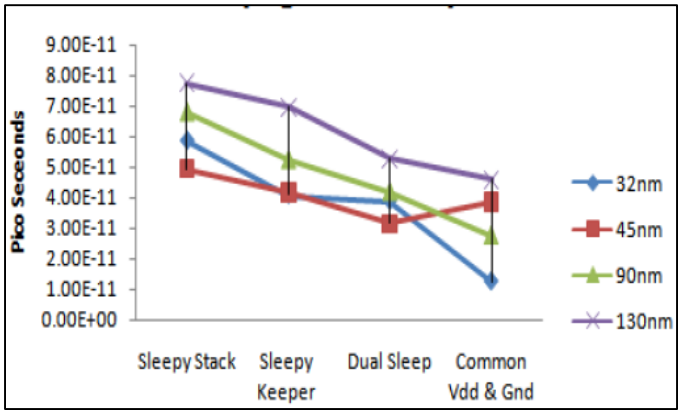

Fig. 2.1: Propagation Delay Comparison

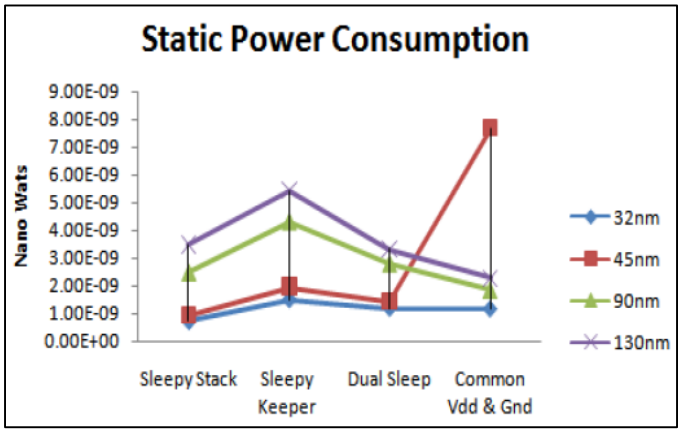

Fig. 2.2: Static Power Consumption Comparison

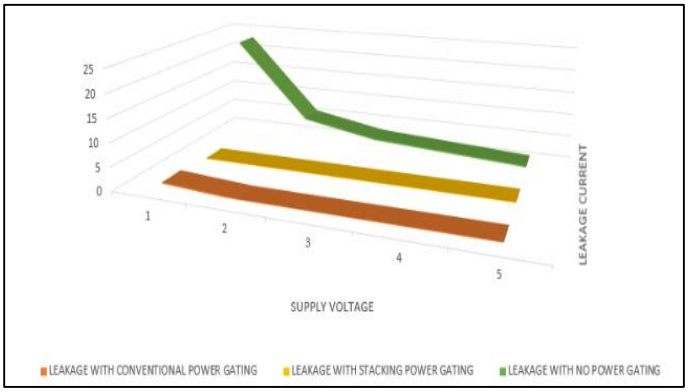

Fig. 2.3: Comparison between Stacking and Conventional Power Gating

IV. PROPOSED METHOD

Each of the methods discussed had their advantages and trade-offs. After thorough analyses we have come to a consensus that a combination of two techniques i.e. stacking power gate and novel common Vdd and GND would probably provide efficient reduction in delay as well as save the state in both modes and also reduce the propagation delay significantly. The pull down network reduces the ground bounce noise and the combination of pull up and pull down helps in saving the logic state.

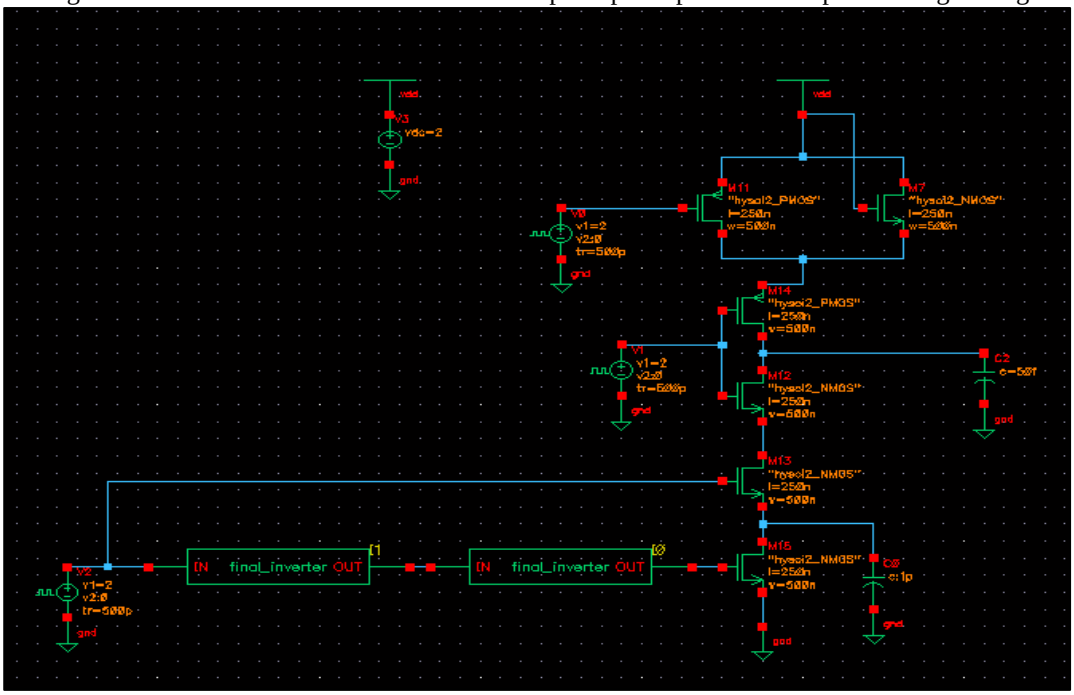

Fig. 3.0: Schematic of the Proposed Technique

To reduce ground bounce noise, we use have to separate the logic circuit from the Gnd for a short delay time, which equals the transition time. We have used two inverters to add the required delay in the circuit, without changing the logic. We used this principle in our proposed technique to see if it would combine the gains of the two studies.

From our simulations on Cadence, we have studied its behavior under transitient, noise and DC analysis. We see that it manages to suppress noise input noise, and we see an almost perfectly zero output noise. Transient response shows how the logic remains unfazed by additional power gating scheme. We however were not able to study the effects of propagation delay, power and area overhead that this scheme would introduce. But previous studies are conclusive enough for us to say that this scheme would provide the necessary gains in terms of power and noise reduction, which are necessary to keep in check at low architecture sizes [10-13]. Future scope would be to check the accuracy rates under various other conditions, which was not possible due to lack of proper resources.

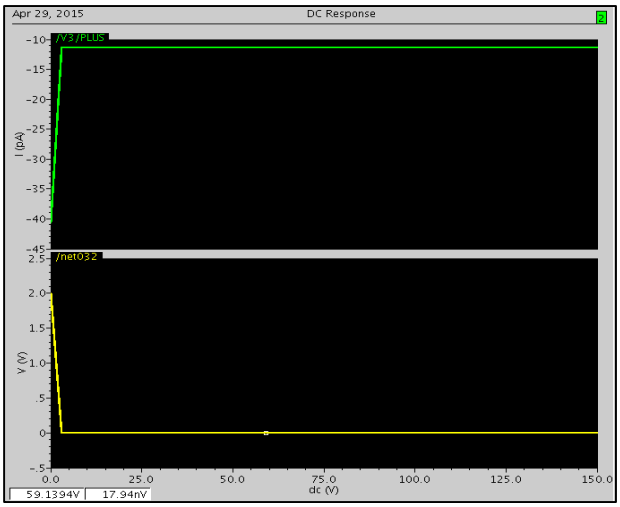

Fig. 3.1: DC Response of the Proposed Technique

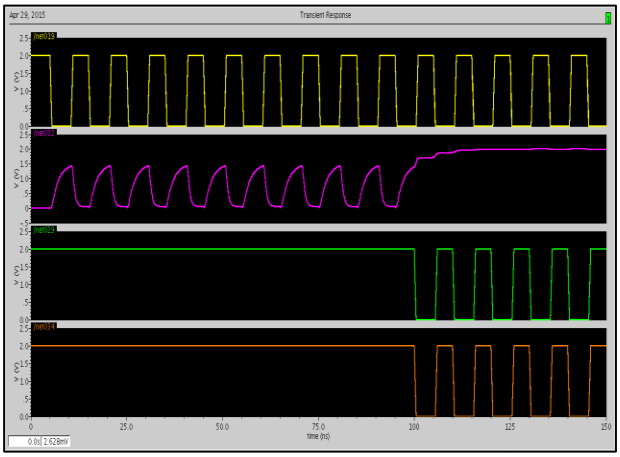

Fig. 3.2: Transient Response of Proposed Technique

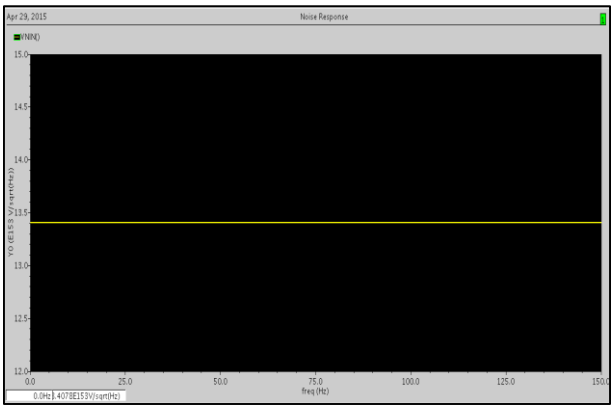

Fig. 3.3: Input noise

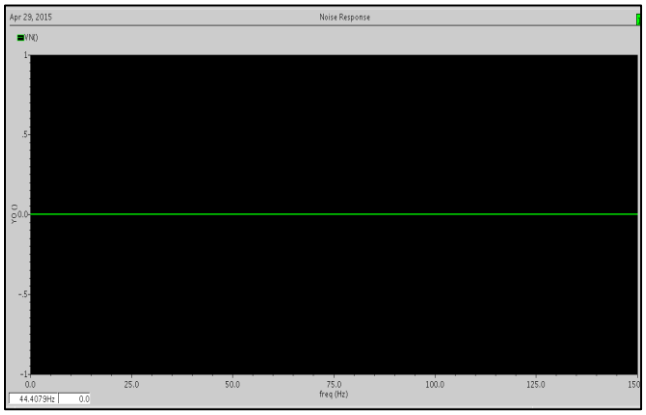

Fig. 3.4: Output Noise of the Proposed Technique

V. CONCLUSIONS

Power gating provides an important means to reduce power consumption in all of the future designs, since we will be going for smaller transistor sizes. However, power gating is not to be confused with clock gating, which is to reduce dynamic power consumption. In this paper we provide our analysis and study on various schemes introduced to us. We compare their performance over various aspects of static power, dynamic power, area, propagation delay etc. We also studied an important phenomenon which is present at a nano-meter scale i.e., ground bounce noise. Techniques to curb it were analyzed and used to propose a novel scheme for both power and noise reduction.

Our scheme takes the positive aspects of all the designs discussed and extrapolates it to show a new approach that can be taken to resolve power gating in modern circuits.

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