Seven Level Cascaded Multilevel Inverter for Power Quality Improvement in Induction Motor

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Abstract

Induction motors are the workhorses of any industry. The speed control of induction motor is mainly done through Variable Frequency Drives (VFD). The VFD includes IGBT or MOSFET based voltage source inverter which is fed from a rectifier. The output AC of the inverter contains more harmonic content and has square waveform. However sinusoidal PWM technique is used to get much more sinusoidal output AC. But the frequent switching of the switches will result in increasing the harmonic content which in turn increases the size of the output filter. To overcome this, a cascaded multilevel inverter is proposed to reduce the harmonic content and improve the power quality. The cascaded multilevel inverter produces nearly sinusoidal output compared to sinusoidal PWM switching. The common configuration of cascaded multilevel inverter includes separate DC sources for each H-bridge. The proposed 3 phase cascaded multilevel inverter has only one DC source. By choosing the adequate switching angles and appropriate carrier frequency, harmonics can be eliminated in the output waveform. Appropriate choice of a fundamental frequency switching pattern can produce a nearly sinusoidal output thereby improving the power quality. In this work, the aim to study the performance of an induction motor, which is used as a medium.

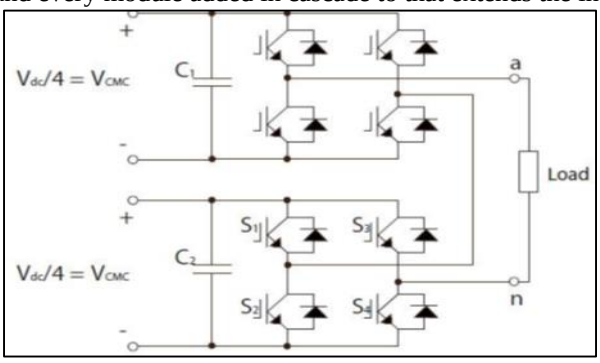
Keyword- Hybrid Cascaded Multilevel Inverter, Total Harmonic Distortion, Sinusoidal Multicarrier Pulse Width Modulation, In-Phase Disposition

I. INTRODUCTION

For the better quality of power the voltage and current waveforms should be sinusoidal, but in actual practice it is somewhat non-sinusoidal and this phenomena is called Harmonic Distortion. Voltage Harmonic Distortion which is generally present in supply of power from utility. The distortion in current waveform is called as current harmonic distortion which is generally injected by the nonlinear loads to the supply of utility and corrupts it.

II. HYBRID CASCADED SEVEN LEVEL INVERTER

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. It uses cascaded full-bridge inverters with separate DC-sources to buildup the stepped waveform. Each full-bridge can be seen as a module and it is only these modules that build up the Cascaded Multilevel Inverter topology. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. It should be noted that, unlike the diode-clamped and flying-capacitor topologies, isolated sources are required for each cell in each phase. In some systems these sources may be available through batteries or photovoltaic cells, but in most drive systems transformer/rectifier sources are used. The figure 4.6 shows the circuit diagram of the five level cascaded multilevel inverter. One full-bridge module is itself a three-level Cascaded Multilevel Inverter, and every module added in cascade to that extends the inverter with two voltage levels.



Every full-bridge can create the three voltages levels. In a full-bridge module to get positive voltage, the switches S1 and S4 are turned on, for negative voltage, the switches S2 and S3 are turned on. The zero voltage is achieved by turning on the two upper halves switches of the full-bridge (S1 and S3) or the two lower half switches (S2 and S4). Together with several full-bridges a stepped waveform can be generated. The Cascaded Multilevel Inverter is capable of producing the total voltage source magnitude in both positive and negative direction while many other topologies can only put out half the total DC-bus voltage source magnitude.

A. Features of Cascaded H-Bridge Multilevel Inverter

Compared to the Diode Clamped and Capacitor Clamped Multilevel Inverter the Cascaded Multilevel Inverter requires fewer components, all voltage level requires the same amount of components but the number of sources are higher. For an _n‘ level inverter, number of sources s = (n-1)/2. The number of sources _s‘ is also equal to the number of full bridge modules. Every full-bridge module has four diodes and four switches in turn giving the Cascaded Multilevel Inverter _4s‘ diodes and switches. When making a three-phase inverter with the Cascaded Multilevel Inverter topology the number of components gets multiplied by three for all components since there is no common DC-bus to share.

B. Advantages of Cascaded H-Bridge Multilevel Inverter

1) The regulation of the DC buses is simple.
2) Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.
3) Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
4) Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers

C. Disadvantages of Cascaded H-Bridge Multilevel Inverter

1) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
2) Needs separate DC sources for real power conversions, and thus its applications are somewhat limited

D. In-Phase Disposition

In this scheme of level shift modulation, each carrier wave have same amplitude, frequency are in phase but their levels are shifted by their peak amplitude. In the similar way for an _n‘ level inverter, the _n-1‘ carriers are used and each has a peak-to-peak value of 2/(n-1).

Thus for a seven level inverter, this scheme has six carrier waves having amplitude of 0.33V. The magnitude of first carrier wave above zero will vary from 0 to 0.33V. The magnitude of second carrier wave will vary from 0.33V to 0.66V. The magnitude of third carrier wave will vary from 0.66V. to 1.0V. Similarly for the three carrier waves below zero, the magnitudes vary from zero to -0.33V, -0.33 to -0.66V and -0.66V to -1.0V respectively. The figure 5.2 shows the In-Phase Disposition PWM scheme for a seven level cascaded multilevel inverter.

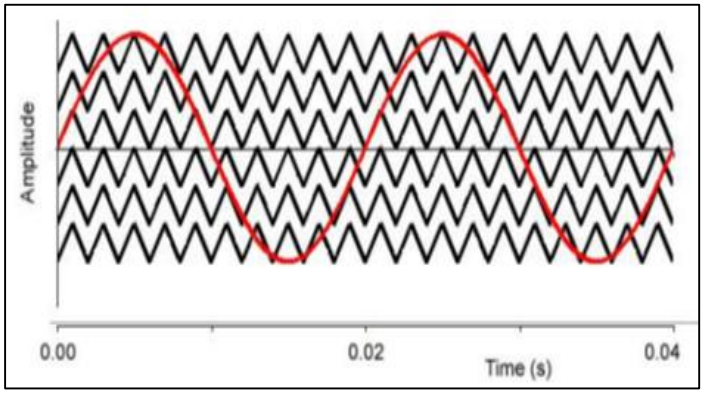


Fig.1.1: In-Phase Disposition Modulation for seven level cascaded multilevel inverter

E. Modified In-Phase Disposition

In this scheme, modified version of In-Phase disposition is used. The modified version has only three carrier waves having peak amplitude of 3V and frequency of 1800 Hz. The control signal used is a rectified sinusoidal signal of frequency 50 Hz and whose amplitude is determined by the desired modulation index. The three carrier waves have magnitude varying from 0 to 3V, 3V to 6V and 6V to 9V. In this modified version, the carriers below zero are avoided. A rectified form of the sinusoidal modulating signal is used instead of pure sinusoidal wave. The pulses for the positive half cycle of the output voltage are generated by comparing the carrier waves and the odd half cycle. The pulses for negative half cycle of the output voltage are generated by comparing the carrier waves and even half cycle. The pulses thus generated are given to six switches of the proposed seven level hybrid cascaded multilevel inverter. The figure 5.5 shows the Modified In-Phase Disposition and the generated switching pulses

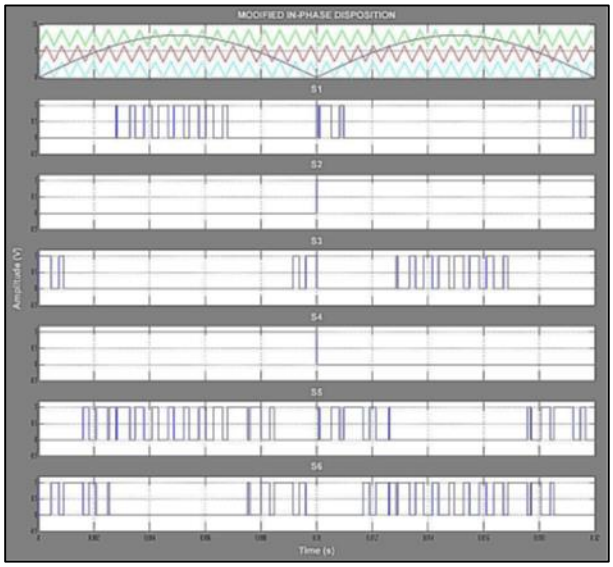


Fig.1.2: Modified In-Phase Disposition for proposed 7 level cascaded multilevel inverter

III. PROPOSED SEVEN LEVEL HYBRID CASCADED MULTILEVEL INVERTER

The MATLAB model of the one phase of a three phase seven level multilevel inverter is shown in figure 6.1. The inverter consist of a H—bridge and two bidirectional switches. The switches S1, S2, S3, S4 forms the H-bridge. The switch S5 together with diodes D1, D2, D3 and D4 forms one bidirectional switch. Similarly, the switch S6 together with diodes D5, D6, D7 and D8 forms the second bidirectional switch. The capacitors C4, C3, C5 forms a voltage divider. The input DC voltage, VDC, which is given across terminal 1 and 4 is divided into three equal voltages, VDC/3, across each capacitor. These three voltages is then utilized to generate the seven level waveform. Proper switching of the inverter can produce seven output-voltage levels (0, +Vdc/3, +2Vdc/3, +Vdc, -Vdc/3, -2Vdc/3,-Vdc).

IV. WORKING

The proposed inverter operation can be divided into seven switching states, as shown in the Table 6.1.
To obtain + Vdc: S1 is ON and S4 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is + Vdc.
To obtain + 2Vdc/3: The bidirectional switch S5 is ON and S4 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is + 2Vdc /3.
To obtain + Vdc /3: The bidirectional switch S6 is ON and S4 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is + Vdc /3.
To obtain Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1and S2 are ON, and all other controlled switches are OFF, the voltage applied to the load terminals are zero.
To obtain - Vdc /3: The bidirectional switch S5 is ON and S2 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is - Vdc /3.
To obtain -2Vdc/3: The bidirectional switch S6 is ON and S2 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is - 2Vdc /3.
To obtain - Vdc: S2 is ON and S3 is ON. All other controlled switches are OFF, the voltage applied to the load terminals is – Vdc.

Vo	S1	S2	S3	S4	S5	S6
Vdc	On	Off	Off	On	Off	Off
2 Vdc/3	Off	Off	Off	On	On	Off
Vdc/3	Off	Off	Off	On	Off	On
0	On	On	On	On	Off	Off
-Vdc	Off	On	Off	Off	On	Off
-2 Vdc/3	Off	On	Off	Off	Off	On
-Vdc/3	Off	On	On	Off	Off	Off

Table 1.4: Switching States of the Proposed Inverter

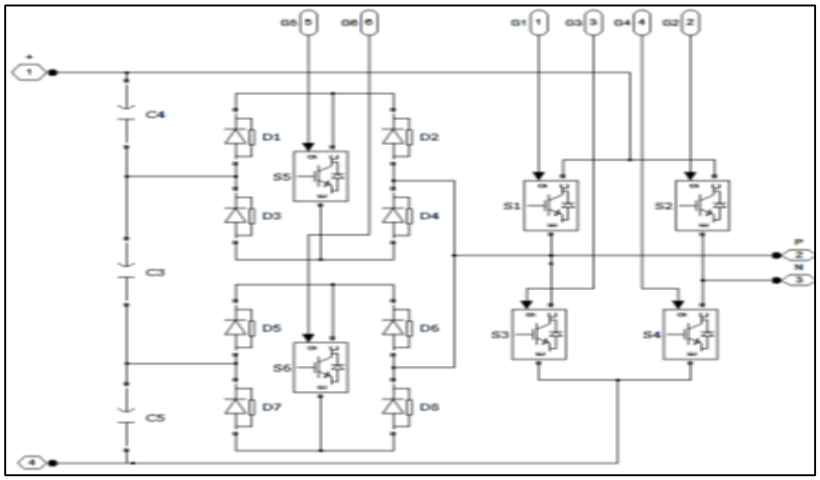


Fig. 1.3: MATLAB Model of the Inverter

The inverter switches are triggered using Sinusoidal multi carrier PWM technique as discussed in previous chapter. In-Phase Disposition technique is employed in this inverter. The carrier frequency used is 1650 Hz, and the control signal corresponding to the required speed of the motor in generated automatically. Pulses thus generated by comparison of the carrier wave and control signal is then fed to logic circuitry to generate the final pulses for the switches. The final pulses are given to the terminals G1, G2, G3, G4, G5 and G6 respectively.

V. FEATURES

One peculiarity of this proposed cascaded inverter is that it requires only one DC source compared to other topologies of cascaded inverters. This specialty makes this inverter suitable for variable frequency drives.
Other feature about this inverter is that the number of switches is very less compared to other topologies which makes the inverter cheaper.
The reduced number of switches will also results in reduced switching losses. The switching signals can be easily generated and complex switching circuitry can be avoided. This results in easy control of the inverter.

VI. MATLAB MODEL

The proposed converter was simulated in MATALB/Simulink. The MATLAB model is shown in figure 7.1. The converter was given 400V, 3-phase, 50Hz input. The input is then given to a 400V / 170V three phase step down transformer. Step down of voltage is done in order to maintain the output line to line voltage at 400V. The step downed voltage is then given to diode bridge rectifier.

The output of the rectifier is then given to each phase of the seven level multilevel inverter. The output of each phase of the inverter is seven level voltage with amplitude 240V. The inverter switches is operated using multicarrier PWM technique. The sinusoidal control signal is generated depending upon the reference speed set by the user. The PWM scheme uses 3 carrier waves each having same amplitude and frequency but clamped at different voltage levels. The pulse is then generated by comparing the sinusoidal control signal and the triangular carrier wave. These pulses are then given to the switches of the inverter which produces the seven level waveform of required frequency. The output of the inverter is then given to the 3 phase squirrel cage induction motor. The details of the motor used is given in table 7.1

SPECIFICATION	*RATING*
RATED VOLTAGE	*400 V*
RATED CURRENT	*63 A*
RATED SPEED	*2955 RPM*
FREQUENCY	*50 Hz*
PHASE	*3*
NO. OF POLES	*2*

Table 7.1: Details of the motor used

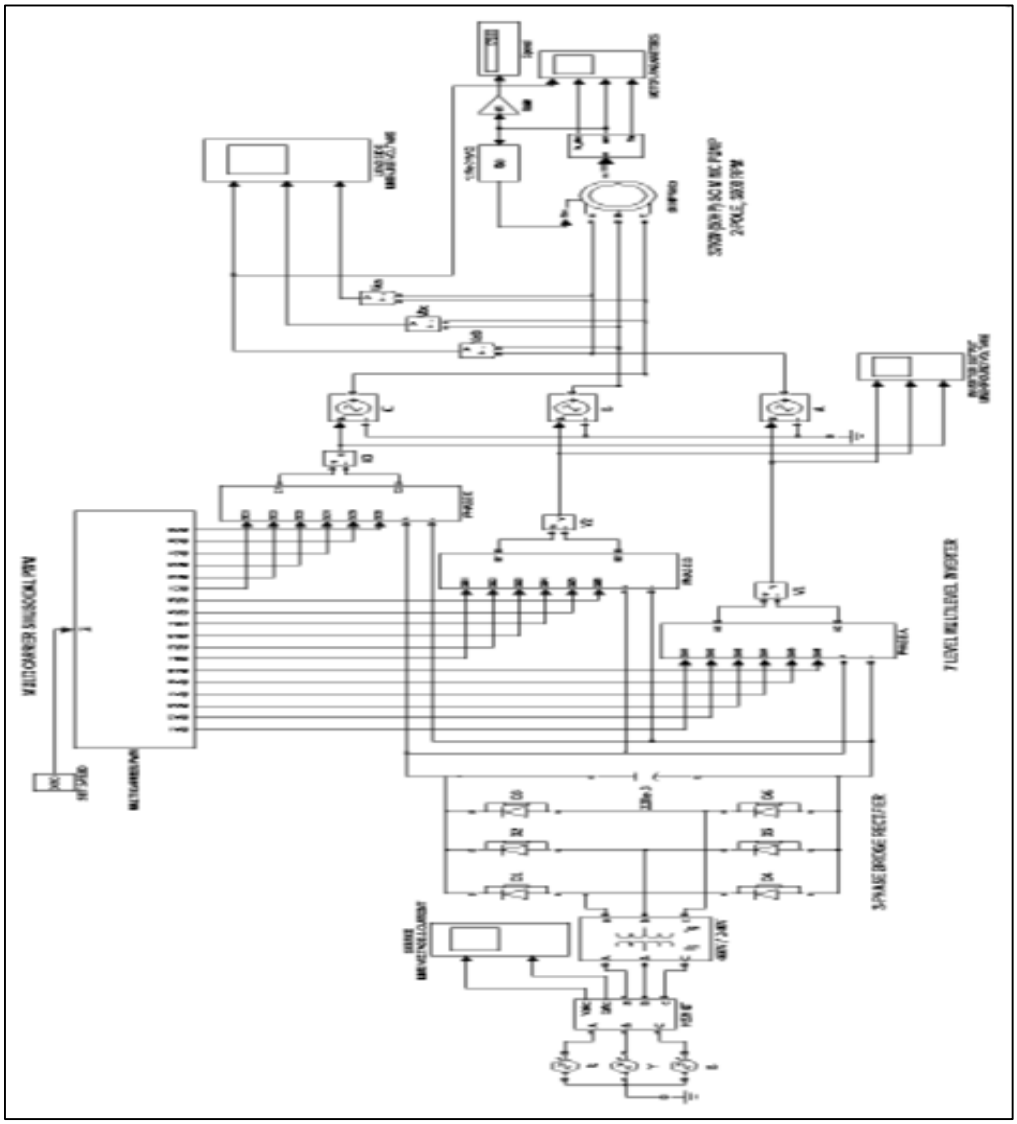
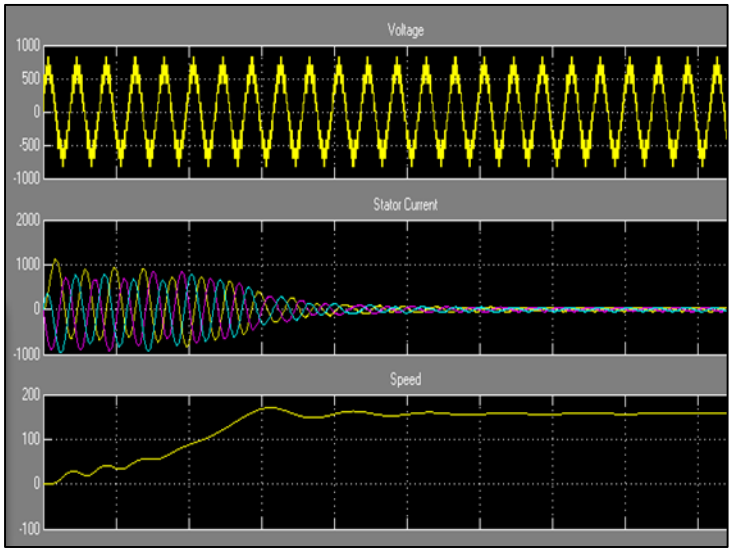
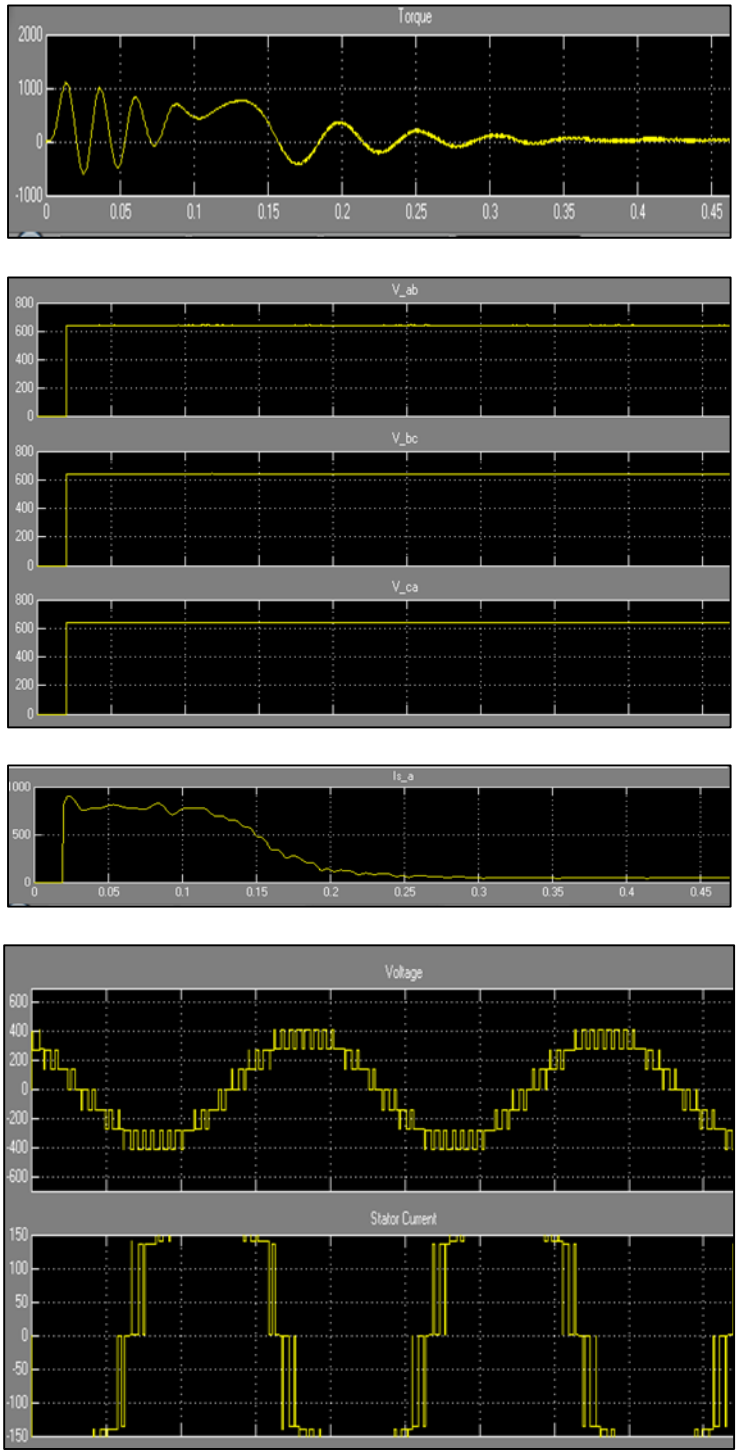


Figure. 1.5: shows the MATLAB model of the proposed variable frequency drive

VII. SIMULATION RESULTS





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