Design of 32 Bit Vedic Multiplier using Carry Look Ahead Adder

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Abstract

The digital architecture is mainly used in all type of real world application architectures and thus the architecture modify based on enhancement purpose. The VISI is to optimize the any type of digital architecture. Multiplication is an important fundamental function in arithmetic logic operation. Computational performance of a DSP system is limited by its multiplication performance and since, multiplication dominates the execution time of most DSP algorithms. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculation based on 16 Sutras. Our work is to develop the 32 –bit Vedic multiplier architecture using carry look ahead adder technique.

Keyword- Vedic Multiplier, Carry Look Ahead Adder

I. INTRODUCTION

A. Multiplication

The speed of a processor, determines its performance. High speed processing is an essential requirement for all the systems. Multiplication is a significant operation in Digital signal processors and ALU, and thus the demand for high speed multiplication is continuously increasing in modern VI.SI design.

Multipliers like booth multiplier, Modified Booth Multiplier, and array multipliers were considered for high speed multiplication, but these multipliers involve large number of intermediate steps, which reduces their speed with increase in the number of bits. For high speed multiplication as well as to increase the performance of multiplier.

II. EXISTING SYSTEM

In Existing system of hardware- level approximation by introducing the partial product perforation technique for designing approximate multiplication circuits. Here proved in a mathematically rigorous manner that in partial product perforation, the imposed errors are bounded and predictable, depending only on the input distribution. Approximate hardware circuits, contrary to software approximations, offer transistors reduction, lower dynamic and leakage power, lower circuit delay, and opportunity for downsizing. The compression operation based on the dadda multiplier function to reduce the circuit complexity level.

III. PROPOSED SYSTEM

The proposed system is used to reduce the carry propagation time and to optimize the hardware complexity level for 32 bit Vedic multiplier operation. The proposed system is to implement vertical and cross-wise equation based logical 32 bit multiplier operation.

A. Vedic Mathematics

Swami Bharati Krishna Tirtha, called a set of 16 Sutras (aphorisms) and 13 Sub-Sutras (Corollaries) from the Atharva Veda. He developed method and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics. In Vedic Mathematics partial products are generated in parallel, which increases the speed of operation. In this paper we are proposing a design for accumulation of these intermediate products, with minimal delay Multiplication if an operation much needed in Digital Signal Processing for various applications.

This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryabgbhyam, a sutra from Vedic Math for multiplication.

B. Vedic Multiplier

This paper presents a high speed 8 x 8 bit Vedic Multiplier architecture which is the quite different from the conventional method of multiplication like add and shift. The most significant aspect of the proposed method is that the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed integrated circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool Xilinx ISE. Finally the results are compared with Conventional multipliers to show the significant improvement in its efficiency in terms of Path delay (speed).

The high speed processor requires high speed multipliers and the Vedic Multiplication technique is very much suitable for this purpose Multipliers are extensively used in Microprocessors, DSP and communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of high speed multiplier is increasing as the need of high speed processors are increasing. Higher throughput arithmetic operation.

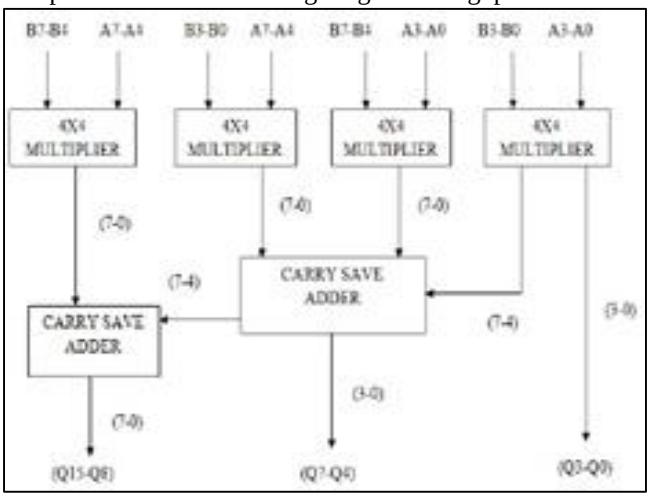
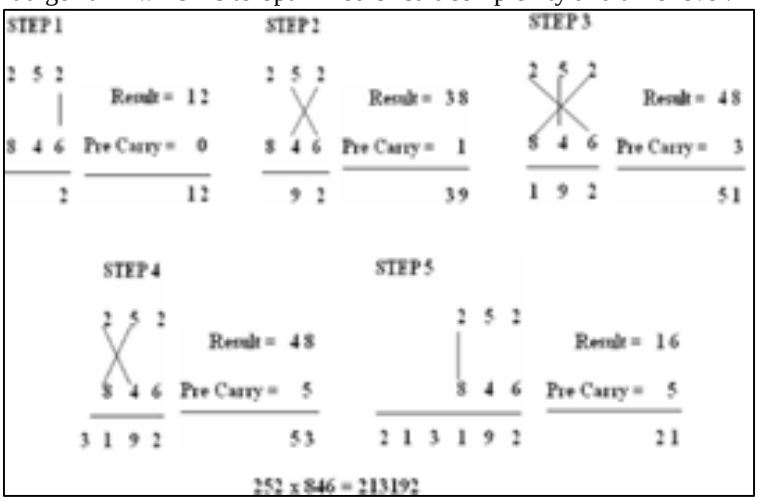


Fig. 1: Block Diagram of Vedic Multiplier

C. Multiplication Algorithm

This algorithm is very efficient algorithm which is to optimized circuit complexity and time level.



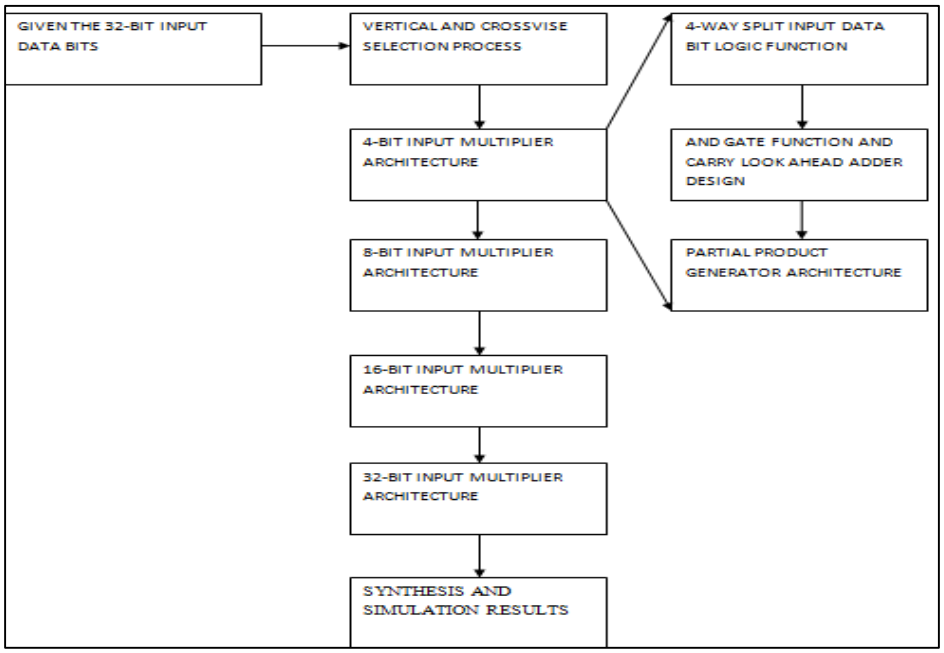
The proposed system is to modify the PPG unit addition process and to optimize the carry selection processing time. The carry selection time is to be reduced. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift.

Vedic mathematics, which simplifies arithmetic and algebraic operations, has increasingly found acceptance the world over. Experts suggest that it could be a handy tool for those who need to solve mathematical problems faster by the day. It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square roots and cube roots. Even recurring decimals and auxiliary fractions can be handled by Vedic mathematics.

The multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. By adapting the Vedic multiplier, structure. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent this power of multiplier. It can easily be increased by increasing the input and output data bus

width since it has a quite a regular problems to avoid catastrophic device failures. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequency.

D. Flow diagram



E. Carry Look Ahead Adder

A Carry Look Ahead Adder or Fast adder is a type of adder used in digital logic. A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits.

The carry Look Ahead Adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder.

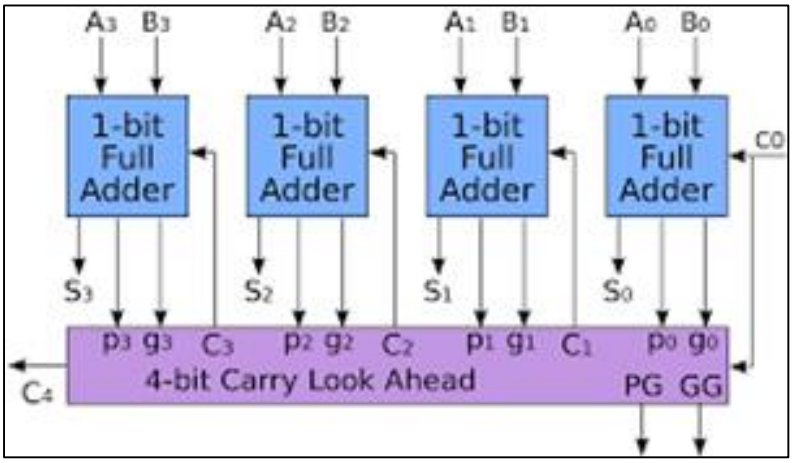


Fig. 2: Carry Look Ahead Adder

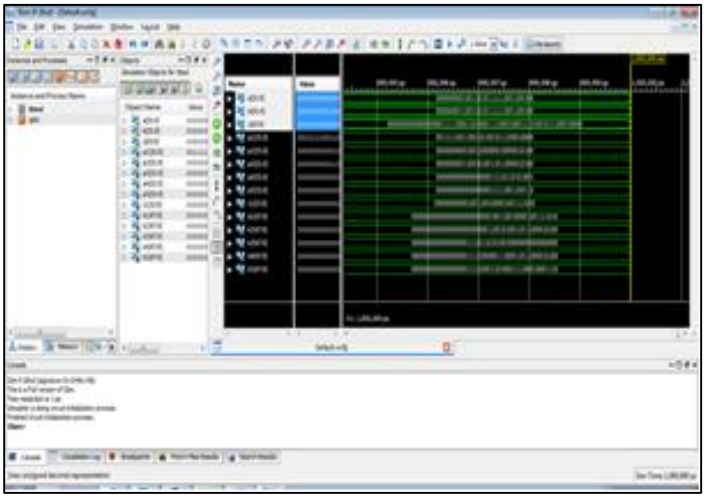
The adder section is to be modified using the Carry look ahead adder process and to optimize the adder architecture. The Carry look ahead adder unit is to reduce the transform function due to the transmission time. The transforming operation is mainly focused by the carry selection process and to reduce the number of Gates into transform architecture. To reduce the power consumption level and the system speed to be high. This modified architecture is used to the more applications.

F. 32 bit Vedic Multiplier Architecture

Our work is to modify the 32-bit multiplier architecture using Vedic mathematics technique. This technique is to implement the vertical and cross-wise equation based process. First we design a 4-bit multiplication operation and to develop the 8-bit multiplication process using 4bit multiplication result. Finally we design a 32 bit multiplier architecture using a 4-bit, 8-bit and 16-bit multiplication process. This structure is to reduce the complexity and time level.

G. Performance and Analysis

The multiplier architecture is mainly used to the ALU UNIT. Because the architecture optimization process is only possible in the VLSI domain. The VHDL language is mainly used to the improve the accuracy compare to another type of process. The XILINX 14.2 software is consists the more library function compare to the previous hardware software. Our process was developed in VHDL language using XILINX software. It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square roots and cube roots. Even recurring decimals and auxiliary fractions can be handled by Vedic mathematics.



H. Result Analysis

Parameters	*Urdhava*	*Nikhilam*
Delay(ns)	*20.33ns*	*18.125*
Memory(kb)	*150964*	*151988*
No.of.slices used	*67 out of 4696*	*91 out of 4656*
No.of.IOB bonds	*32 out of 158*	*33out of 158*

IV. CONCLUSION

This paper presents a highly efficient method of multiplication– "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for modular multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed new Vedic multiplier is found to be less as compared to other multiplier. Hence our motivation to reduce delay is finely fulfilled. Therefore, we observed that the new Vedic multiplier is much more efficient than Array and conventional multiplier in terms of execution time (speed). It is used for Digital Signal Processing application. The Proposed Multiplier designs can be used in applications with minimal loss in output quality while saving significant power and area.

REFERENCES

[1] Suganthi Venkatachalam and Seok – Burn Ko, IEEE JOURNAL"Design of Power and Area Effcient Approximate Multiplier December 2016".
[2] P. Ram Sirisha, Dr.A.M. Prasad, IEEE JOURNAL"Design and Performance Analysis of 32 bit Array Multiplier using optimized Carry Select Adder September 2015".
[3] Anushukhare Ashish, Raghwanshiruchi Gupta, IEEE JOURNAL"Vedic ALU using Area optimized Urdhva Triyambakam Multiplier 2014".
[4] Pratisha Rai, Shailendra Kumar, Prof.(Dr.) S.H. Saeed, IEEE JOURNAL"Design of floating point multiplier using Vedic Aphorims 2014".
[5] Sudhanshu Shekhar Pandey, Amit Bakshi, Vikash Sharma, IEEE JOURNAL"128 bit Low Power and Area Efficient Carry Select Adder May 2013".
[6] N. Vijayabala and T.S. Saravana Kumar, IEEE JOURNAL "Area minimization of Carry Select Adder using Boolean algebra July 2013".

[7] T. Ratna Mala, R. Viney Kumar, T. Chandra Kala, IEEE JOURNAL "Design and Verification of Area efficient High Speed Carry Select Adder November 2012".
[8] S. Ramachandran, Kirti. S. Pande , IEEE JOURNAL"Design, Implementation and Performance Analysis of an Integrated Vedic Multiplier Architecture 2012".
[9] Rangharajan Vemkatesan, Amit Agarwal, Kaushik Roy and Anand Raghunathan, IEEE JOURNAL "Modeling and Analysis of circuits for Approximate Computing 2011".
[10] C.N. Marimuthu, Dr.P.Thangaraj, Aswathy Ramesan, IEEE JOURNAL"Low Power Shift and ADD Multiplier Design June 2010".