Analysis of Carry Select Adder using Different Logic Styles

Fincy Mol
Assistant Professor
Department of Electronic and Communication Engineering
Prince Shri Venkateshwara Padmavathy Engineering College, Tamilnadu,India

Saranya Tv
Assistant Professor
Department of Electronic and Communication Engineering
Prince Shri Venkateshwara Padmavathy Engineering College, Tamilnadu,India

Shalini M
Assistant Professor
Department of Electronic and Communication Engineering
Prince Shri Venkateshwara Padmavathy Engineering College, Tamilnadu,India

Abstract

Carry Select Adder (CSLA) is one of the fastest adder used to perform fast arithmetic operations. In our project, a modified carry select adder is designed by using single Ladner-Fischer (LF) and binary to Excess-1 Converter (BEC) instead of using dual RCA's to reduce the area and delay. The correct sum and carryout signals will be selected by a set of multiplexers. LF adder is a parallel prefix form of carry look-ahead adder (CLA). It is the fastest adder with focus on time and is the common choice for high performance adders in industry. The better performance of LF adder is because of its minimum logic depth and bounded fan-out. In the proposed CSLA, one ripple carry adder (RCA) fed with Cin=0 is replaced by LF adder. The performance of proposed CSLA is analyzed and compared against CSLA design using RCA and BEC. The number of gates used in proposed CSLA is fewer than the CSLA using RCA and BEC. The result shows that area of proposed method is reduced by 25% and delay is reduced by 14%.
Keywords- Fast Arithmetic Operations, Ladner-Fischer, Minimum Logic Depth

I. INTRODUCTION

Adders are generally established in the critical pathway of various building blocks of several microprocessors and various digital signal processing chips. Adders are not only necessary for addition, but also necessary for subtraction, multiplication and division. A very fast and accurate function of digital system is powerfully manipulated by the performance of the resident adders. Power, delay and area are the three most widely used parameters for measuring the performance of a circuit.

There are several types of adders, each one has certain performance. The adders are selected depending on their usage. Carry Select Adder (CSLA) is one of the fastest adders used in many data processing processors to perform fast arithmetic operations. Generally Carry select adders are used for high speed operations [12].

In carry-select adder design, an adder with small number of stages and the adder with large number of stages are performed in same speed [13]. The basic operation of carry select adder is parallel computation. CSLA uses various pairs of RCA to produce partial sum and carry by considering Cin=0 and Cin=1. Final sum and carry are chosen by multiplexers [9]. The creation of Carry select adders contains multiple levels. Depending on the levels, the hardware costs increase.

II. CARRY SELECT ADDER USING RIPPLE CARRY ADDER

CSLA is usually created by one multiplexer and dual ripple carry adders where Ripple carry adders are made by cascading full adders blocks in series. The carry output of preceding stage is directly fed to the carry input of the next stage, in RCA. Even though RCA is the simple and it can be used to add unlimited bit length numbers, it is not very efficient when large numbers of bits are used. One of the main disadvantages of this adder is that when the bit length increases the delay also increases. When a carry signal conversion ripples through all stages of adder chain from the significant bit to the most significant bit, the delay is more. This is approximate by:

$$t= (n-1)\, t_c + t_s \qquad (1)$$

Where t_c is the delay through the carry stage of a full adder, and t_s is the delay to compute the sum of the last stage [5].

All rights reserved by *www.grdjournals.com*

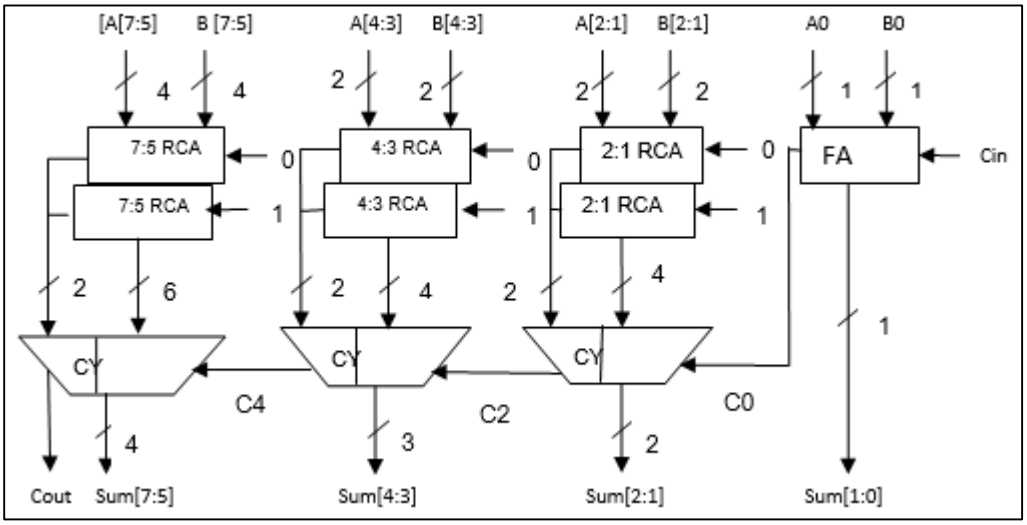


Fig. 1: 8-bit Carry select adder using RCA

Carry select adder is based on the principle to compute sum that is based on assuming input carry from previous stage. One adder determines the sum assuming input carry of 0 while the other determines the sum assuming input carry of 1. Then the actual carry triggers a multiplexer that selects the suitable sum. The main drawback of the regular CSLA is that huge area is necessary for this adder because of the multiple pairs of ripple carry adder. Another drawback is that CSLA is slow since RCA produces more delay.

III. CARRY SELECT ADDER USING BINARY TO EXCESS ONE CONVERTER

In carry select adder using RCA, more area is required due to dual ripple carry adders and also carry out at each stage must ripple. One RCA is replaced with BEC (Cin=1) to diminish delay caused by one of the RCA (Cin=1) and to reduce the area. To replace the N-bit RCA, an N+1 bit BEC is necessary that is the number of bits needed for BEC logic is 1 bit more than the number of bits necessary for RCA. BEC is a circuit that is utilized to add 1 to the input bits. In this circuit, one input of the MUX is B3, B2, B1, and B0 and another input of the MUX is the BEC output. This offers the two results in parallel and based on the control signal, the MUX is utilized to choose either the output of BEC or the direct inputs.

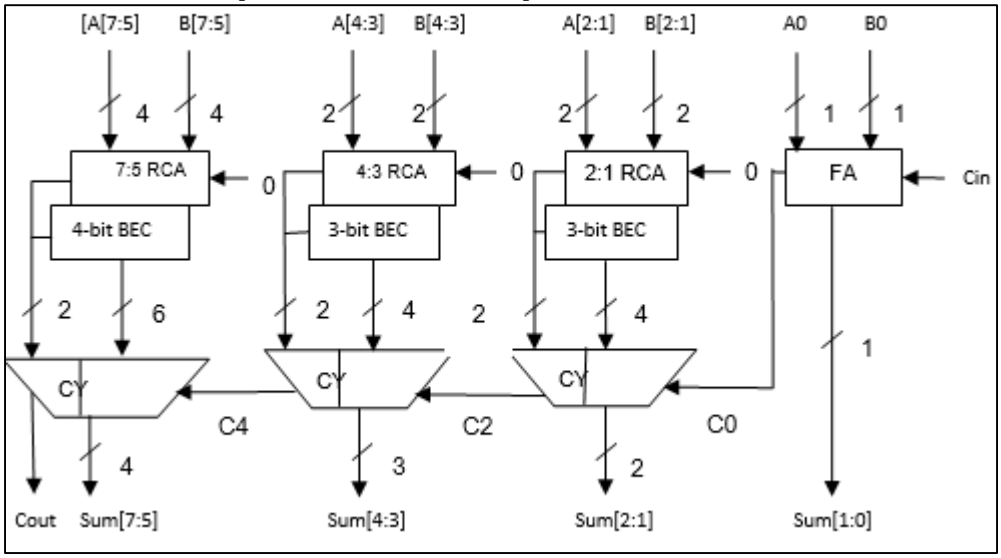


Fig. 2: 8-bit Carry select adder using BEC

Carry Select adder using BEC is shown in fig 5. RCA is used to add the least significant bits and the other blocks are added in parallel together with the given incremented. Multiplexers with less delay are utilized to calculate the final sum after the interim sums and carries are computed. The multiplexer block gets the two sets of input and chooses the final sum according to the select input from the preceding stage. Thus, the use of BEC with MUX attains fast incrementing action with less number of gates. This gives an immense benefit in the diminution of area and total power utilization. Thus, the end result illustrates that Carry Select Adder using BEC is superior to Carry Select Adder using RCA in terms of area and power.

All rights reserved by *www.grdjournals.com*

IV. CSLA USING LF ADDER

The CSLA using LF adder is proposed to optimize the area and delay which is shown in figure. Ladner-Fischer adder is a parallel prefix form of Carry Look-ahead Adder. Ladner-Fischer adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is o (log n). It is the fastest adder with focus on time and is the common choice for high performance adders in industry.

A. Parallel Prefix Adders

The parallel prefix adders are more flexible and are used to speed up the binary additions. Parallel prefix adders are obtained from Carry Look Ahead (CLA) structure. Tree structure form is used to increase the speed of arithmetic operation. Parallel prefix adders are fastest adders and these are used for high performance arithmetic circuits in industries.
The construction of parallel prefix adder involves three stages.

- Pre- processing stage
- Carry generation network
- Post processing

B. Pre-Possessing Stage

In the 1st stage, to each couple of inputs A and B, we need to calculate, generate and propagate signals. These signals are specified by the logic equations (2) & (3):

$$P_i = A_i \text{ xor } B_i \quad (2)$$
$$G_i = A_i \text{ and } B_i \quad (3)$$

C. Carry Generation Network

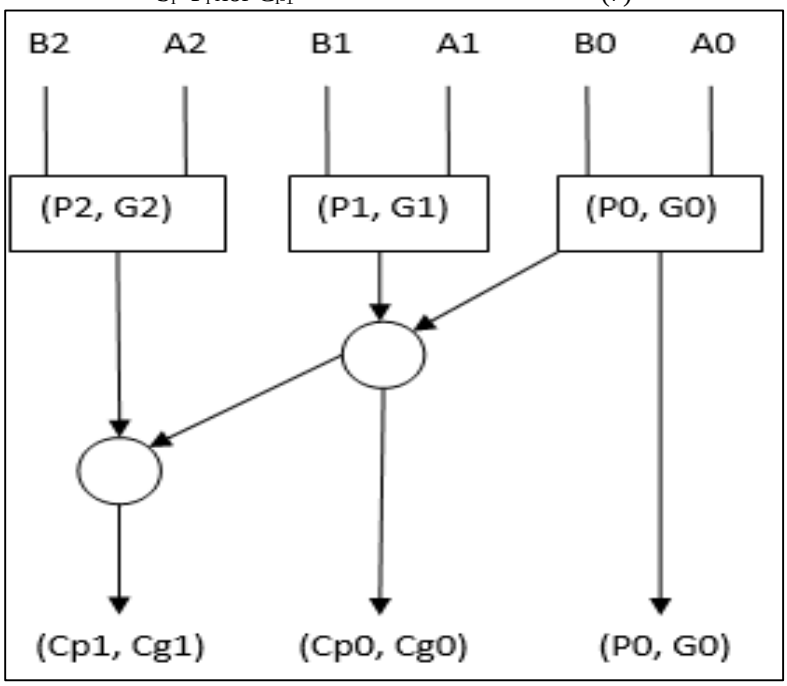
In the 2nd stage, corresponding to each bit, we need to calculate carries. The operations are executed in parallel. After this operation, they are divided into tiny pieces. It makes use of carry propagate and generate as intermediate signals. These signals are specified by the following logic equations (4) & (5):

$$CP_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \quad (4)$$
$$CG_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \quad (5)$$

D. Post Processing

The summing up of input bits is carried out in this stage. It is familiar for all adders and they are calculated by the following logic equations (6) & (7):

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \quad (6)$$
$$S_i = P_i \text{ xor } C_{i-1} \quad (7)$$



$$CP_0 = P_i \text{ and } P_j \quad (8)$$
$$CG_0 = (P_i \text{ and } G_j) \text{ or } G_i \quad (9)$$

The actions involved in figure are specified as follows:

All rights reserved by *www.grdjournals.com*

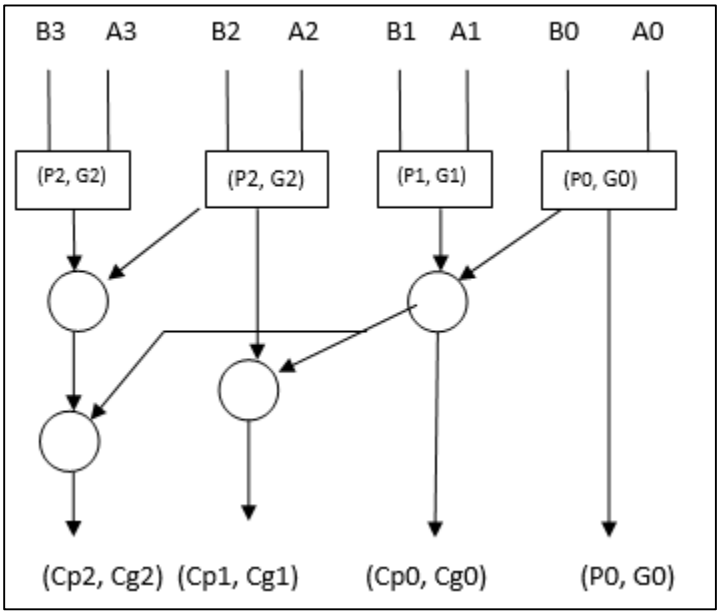


Fig. 4: 4-bit LF adder

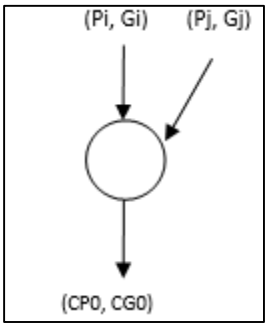


Fig. 5: Carry operator

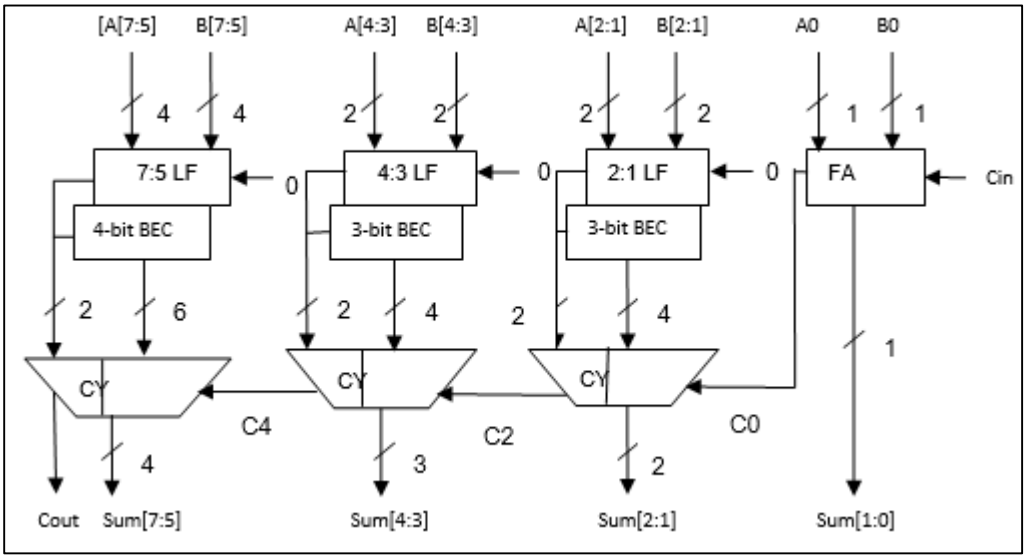


Fig. 6: 8-bit Carry select adder using LF adder

The better performance of Ladner-Fischer adder is because of its minimum logic depth and bounded fan-out. On the other side it occupies large silicon area. This type of adder is based on the attitude to estimate sum that is based on considering input carry from preceding stage. If the carry is equal to 0, then LF adder calculates the sum. Otherwise, BEC calculates the sum. Finally, MUX selects the suitable sum corresponding to the actual carry. Thus, the design of CSLA using LF adder is better than CSLA using BEC and CSLA using RCA.

All rights reserved by *www.grdjournals.com*

V. RESULTS AND DISCUSSIONS

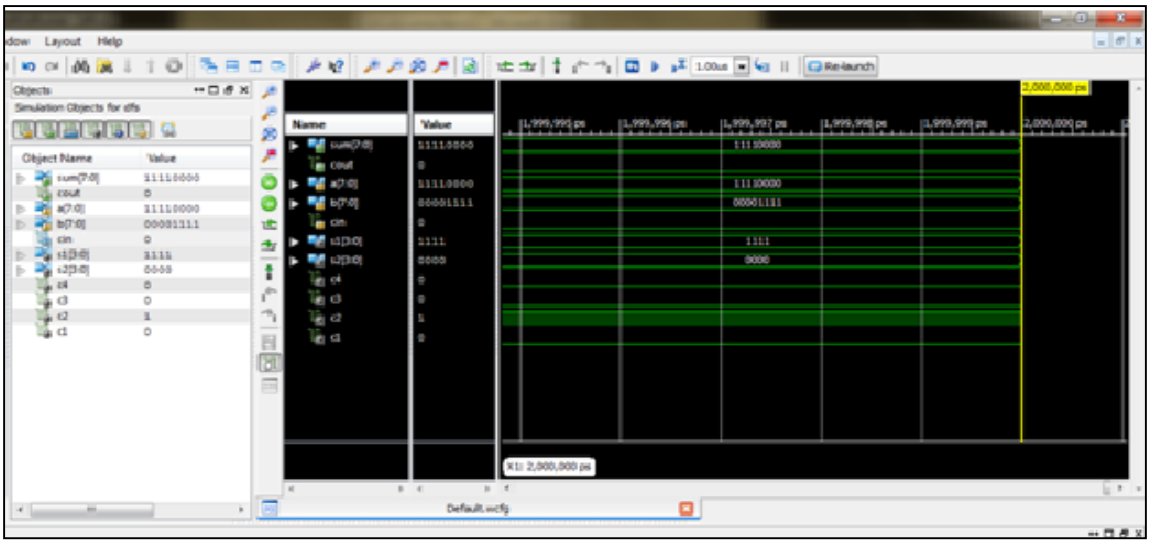


Fig. 7: Verilog output of 8-bit CSLA using RCA

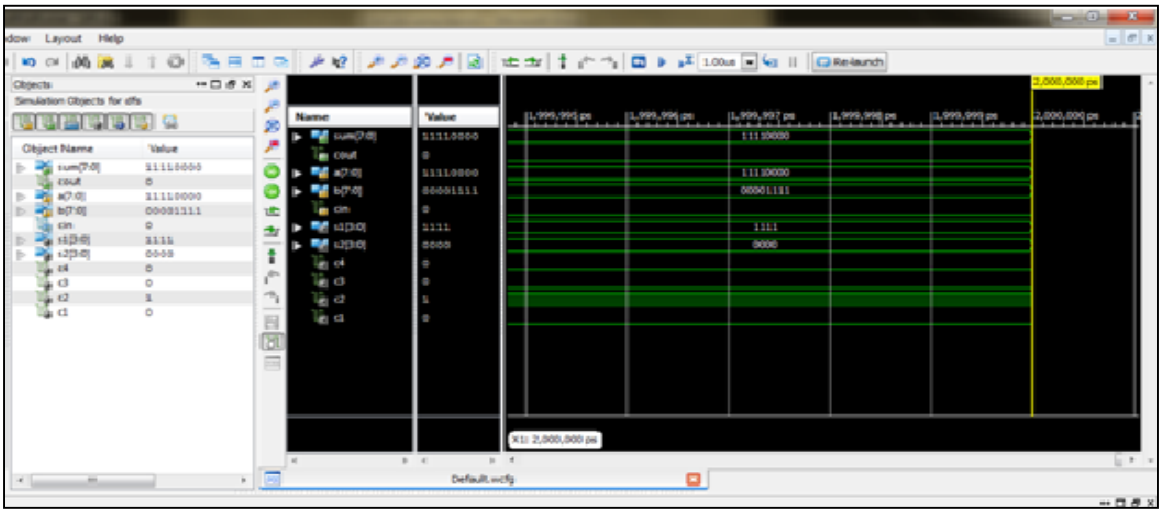


Fig. 8: Verilog output of 8-bit CSLA using BEC

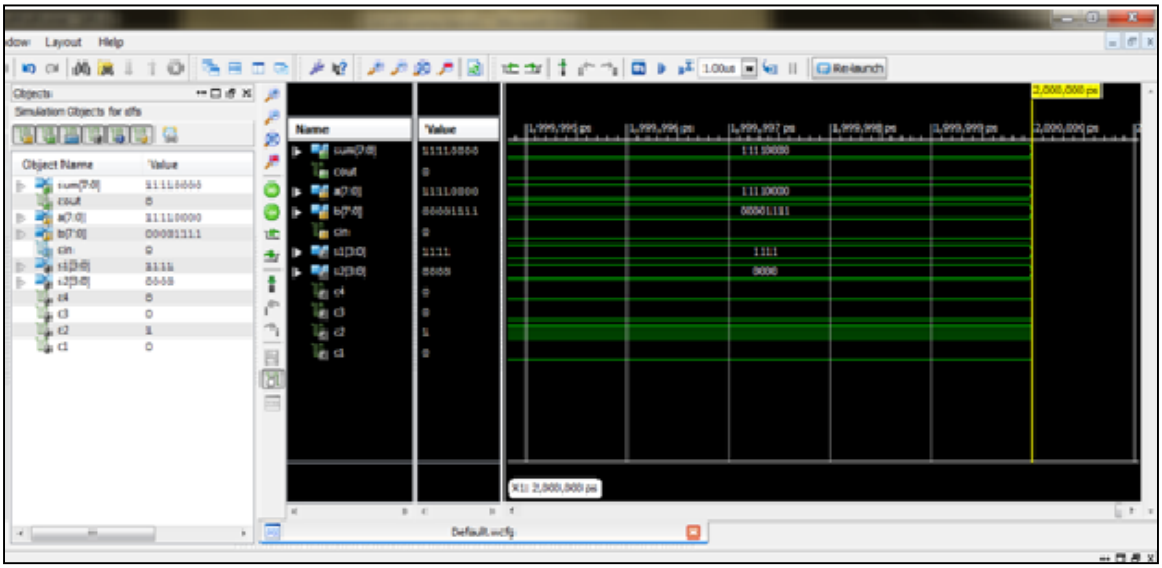


Fig. 9: Verilog output of 8-bit CSLA using LF Adder

All rights reserved by *www.grdjournals.com*

JU5I6L7OUI Project Status			
Project File:	ju5i6l7oui.ise	**Current State:**	Synthesized
Module Name:	uuo	**• Errors:**	No Errors
Target Device:	xc3s100e-5vq100	**• Warnings:**	No Warnings
Product Version:	ISE, 8.1i	**• Updated:**	Sat Feb 21 14:32:37 2015

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	13	960	1%
Number of 4 input LUTs	22	1920	1%
Number of bonded IOBs	26	66	39%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Feb 21 14:32:37 2015	0	0	0
Translation Report	Out of Date	Sat Feb 21 14:29:53 2015	0	0	0
Map Report	Out of Date	Sat Feb 21 14:29:55 2015	0	0	1 Info
Place and Route Report	Out of Date	Sat Feb 21 14:29:58 2015	0	0	1 Info
Static Timing Report	Out of Date	Sat Feb 21 14:30:01 2015	0	0	2 Infos
Bitgen Report	Out of Date	Sat Feb 21 14:00:59 2015	0	0	0

Fig. 10: Design utilization summary of 8-bit CSLA using RCA

xczv Project Status (02/25/2015 - 18:34:38)			
Project File:	yty.xise	**Parser Errors:**	No Errors
Module Name:	xczv	**Implementation State:**	Synthesized (Failed)
Target Device:	xc3s100e-5vq100	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	1 Warning (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values) [-]			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	12	960	1%
Number of 4 input LUTs	21	1920	1%
Number of bonded IOBs	26	66	39%

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Feb 25 18:34:35 2015	0	1 Warning (0 new)	0
Translation Report	Out of Date	Wed Feb 25 18:28:24 2015	0	0	0

Fig. 11: Design utilization summary of 8-bit CSLA using BEC

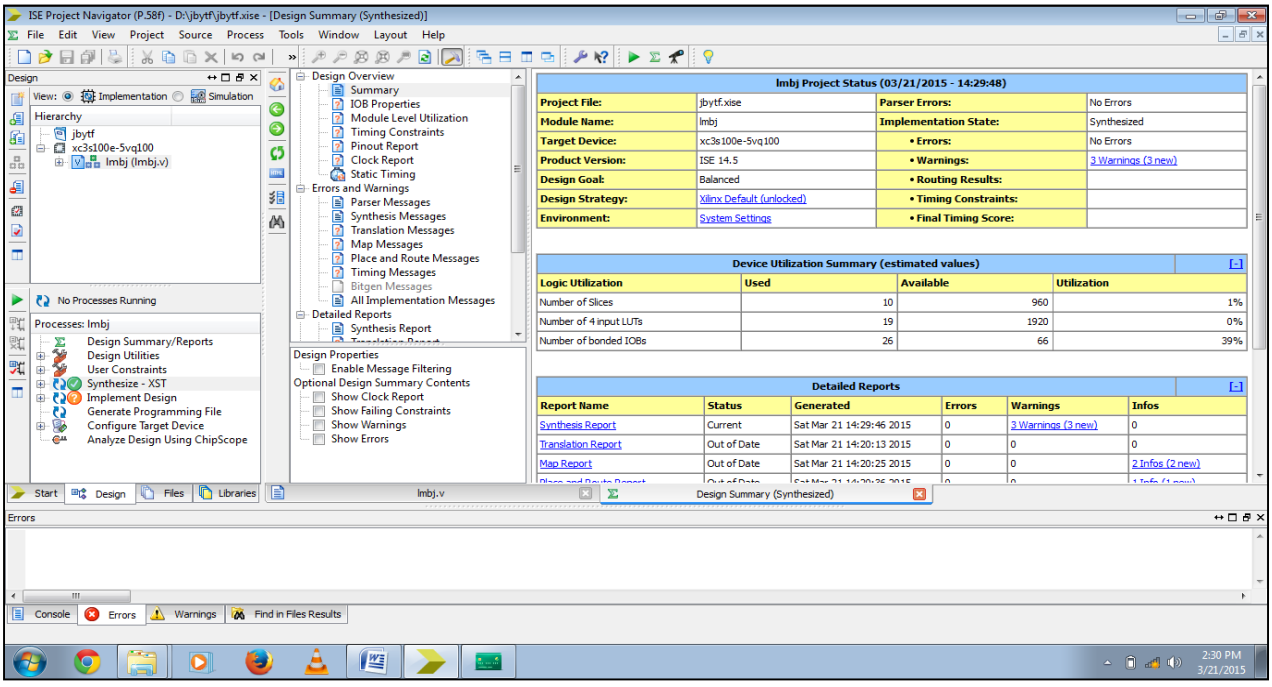


Fig. 12: Design utilization summary of 8-bit CSLA using LF adder

All rights reserved by *www.grdjournals.com*

By comparing the synthesis report for 8-bit CSLA using RCA, 8-bit CSLA using BEC and 8-bit CSLA using LF adder, the area and delay of proposed CSLA is less than other types of CSLA. It is shown in table.

Table 1: Comparison of different CSLA

Adder Type	*No. of LUT's*	*No. of Slices*	*Logic Delay (ns)*	*Route delay (ns)*	*Total delay (ns)*
CSLA using RCA	*22*	*13*	*7.688*	*5.503*	*13.191*
CSLA using BEC	*21*	*12*	*7.335*	*2.958*	*10.293*
CSLA using LF Adder	*19*	*10*	*7.335*	*2.804*	*10.139*

VI. CONCLUSION

In this paper, an efficient approach is proposed to reduce the area and delay of CSLA architecture. The reduction in the number of gates is obtained by simply replacing the RCA with LF adder in the structure. The compared result shows that CSLA using LF adder has lesser area than other types of CSLA. This is because, the number of gates used in the design of LF adder is low. In this design, the delay is reduced to a great extent. Thus the result shows that using proposed method, the area and delay will decrease. Thus, it leads to good alternative for adder implementation for many processors. Further area and delay can be reduced by using LF adder in the place of BEC in the design of proposed CSLA architecture.

REFERENCES

[1] Pakkiraiah Chakali, Madhu Kumar Patnala, "Design of high speed Ladner Fischer based carry select adder", International Journal of soft computing and engineering (IJSCE), ISSN: 2231-2307, vol-3, issue-1, pp.173-176, March 2013.
[2] N.Vijaya Bala and T.S. Saravana kumar,"Area minimization of carry select adder using boolean algebra", International journal of advances in engineering and technology, ISSN: 22311963,vol.6,issue 3, pp.1250-1255, July 2013.
[3] Woopyo jeong, Kaushik roy and Cheng-kok koh,"High performance low power carry select adder using dual transition skewed logic".
[4] Senthil kumar.A and Kousalya devi.A, "VLSI implementation of efficient carry select adder architecture", International journal of advance research in science and engineering IJARSE, vol.No.2, Issue No.4,pp 88-93, April 2013.
[5] Yuke Wang, C.Pai and Xiaoyu Song, "Design of hybrid carry look ahead/ carry select adders", IEEE transactions on circuits and system-2: analog and digital signal processing, vol.49, no.1, January 2002, pp.16-24.
[6] Gangandeep Singh and Chakshu Goel,"design of low power and efficient carry select adder using 3-T XOR Gate", Hindawi publishing corporation advances in electronics, Article Id 564613,pp.1-6, Volume 2014.
[7] Laxman Shanigarapu and Bhavana P. Shrivastava,"Low power and high speed carry select adder", International Journal of scientific and research publications, Vol .3, Issue 8, ISSN 2250-3153,pp.1-9, Aug 2013.
[8] B.Ramkumar and Harish M Kittur, "Low power and area efficient carry select adder", IEEE transaction on very large scale integration (VLSI) systems, vol.20, no.2, pp.371-375, February 2012.
[9] N Dhanunjaya Rao and Ashok Kumar, "FPGA implementation of high performance carry select adder", international journal of advanced research in electronics and communication Engineering (IJARECE), volume 1, issue 6,pp.58-64, Dec 2012.
[10] Sarabdeep Singh and dilip kumar,"Design of area and power efficient modified carry select adder ", International Journal of computer applications (0975-8887), volume 33-no.3, Nov 2011.
[11] Sun yan, Zhang xin and Jin xi," Low-power Carry Select Adder Using Fast All-one Finding Logic".
[12] Gyanesh Savita, Vijay Kumar Magraiya, Gajendra Kulshrestha and Vivek Goyal, "Designing of low power 16-bit carry select adder with less delay in 45nm CMOS process technology", International Journal of Emerging Techno logy and Advanced Engineering, ISSN 2250-2459, ISO 9001:2008, volume 3, Issue 7, pp.250-252,July 2013.
[13] Lakshmanan, Ali Meaamar and Masuri Othman," High-Speed Hybrid Parallel-Prefix Carry-Select Adder Using Ling's Algorithm",IEEE, 2006, pp.598-602.
[14] Amita P. Thankare, Saurabh Agrawal and Vibha Tiwari, "32 bit carry select adder with BEC-1 technique" Proceedings of Sixth IRAJ International Conference, 6th October 2013, Pune, India. ISBN: 978-93-82702-32-0, pp. 127-132.
[15] Yajuan He. Chip Hong Chang and Jiangmin Gu, "An area efficient 64-bit square root carry select adder for low power applications", IEEE, 2005, pp.40824085.
[16] Salivahana and Arivazhagan, "Digital Electronics", third edition.
[17] G.A.Ruiz and M.Granda,"An area efficient static CMOS carry select adder based on a compact carry look ahead unit", microelectronics journal 35, 2004, pp. 939-944.

All rights reserved by *www.grdjournals.com*