Wideband Frequency Synthesizer Implementation using FPGA

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Abstract

Frequency synthesizer is an electronic device that is used for creating a number of frequencies in a large band by using a constant signal from an oscillator. They are used in a lot of devices like Satellites, walkie-talkies, cell phones etc. Direct digital frequency synthesizer (DDFS) is a device which is used to generate a large number of frequencies using electronic technique. Its input is a constant digital signal and it generates a discretionary waveform of different frequencies. It is also known as Numerically Control Oscillator. Its detailed parts are ROM, phase accumulator and phase register. It has some analog parts also like digital to analog converter and a low pass filter. When reference clock is given to NCO, it produces a square signal which advances at each progressive clock. The phase register is used to produce various phases using shift keying etc. The main purpose of this paper is to outline, investigate and to reproduce DDFS using environments like Xilinx, Cadence etc. Currently phase locked loops are in wide use but DDFS provides many advantages over PLL like low noise, low cost, fast settling time and high range of frequencies.
Keywords- Frequency Synthesizer, PLL, HDLs, FPGAs

I. INTRODUCTION

The increasing complexity of wireless communication systems has made Wide Band Frequency Synthesizer an essential component. They are used as frequency synthesizers with precise and convenient digital control in both traditional electronics, such as televisions and AM/FM radios, and modern consumer products among which cellular mobile phone is a striking example. IC fabrication technology advances have made monolithic integration possible. More and more electronic devices can be put on the same chip to reduce the number of external components and then the costs. Therefore, on a single chip, we can accomplish many functions for which we might need to make several chips work together a few years ago. A monolithic PLL is of great interests to wireless communication applications due to both its low cost and convenience to switch between different communication standards. In order to obtain a simple structure, our main focus is on to implement our wide-band Frequency Synthesizer using the minimum number of building blocks. Many of the concepts of DDS are illustrated by the way in which a sine wave is generated. Figure 1 shows a block diagram of a simple DDS function generator. The RAM table holds the values of Sine Functions. The RAM's digital sine output is converted to an analog sine wave by a DAC. The output from DAC unit is filtered by a low pass filter to get a pure sine wave output. The frequency of the sine wave is proportional to the rate at which addresses in the RAM table are changed. The accessing of addresses data are generated by adding a constant to the phase accumulator, these constants are stored in the phase increment register (PIR). Usually, the rate of additions is constant, and the frequency is changed by changing the number in the PIR. To achieve the pure sine wave there should be a large number of samples are required for each cycle of the sine wave generation.

II. RELATED WORK

Qahtan Khalaf OMRAN et al (2013), A low–complexity direct digital frequency synthesizer based on linear interpolation method is presented in this work. The proposed architecture employs a new technique to derive the slope coefficients at the first sample of each segment's interval thereby eliminating the ROM which stores those values. ROM elimination has resulted in significant logic element saving and simplified the whole DDFS structure. The proposed DDFS has been analyzed using MATLAB and tested over the entire Nyquist frequency range. The spurious-free dynamic range (SFDR) of synthesized sinusoid achieved is 84 dBc. The resultant low complexity architecture along with high spectral purity synthesized signal meets the specifications of recent portable battery-driven products [1].

Woogeun Rhee et al (2013), this work gives an overview of fractional- N phase-locked loops (PLLs) with practical design perspectives focusing on a 0Σ modulation technique and a finite-impulse-response (FIR) filtering method. After simulation and hardware results he discussed the Spur generation and nonlinearity issues in the 0Σ fractional-N PLLs. The major application of high-order 0Σ modulation with FIR-embedded filtering is for low noise frequency generation. Also, various architectures of finite-modulo fractional-N PLLs are reviewed for alternative low-cost design, and the FIR filtering technique is shown to be useful for spur reduction in the finite-modulo fractional-N PLL design [2].

Kusum Lata et al (2013), worked on ADPLL that was contribute the great role in advancement in control system and digital communication since 1980. The design of ADPLL with integrated circuit (IC) techniques has made ADPLL very important component. ADPLL is still continuing to give better results. Now a day ADPLL has great contribution in digital communication systems. This work gives basic details of an ADPLL. It provides a brief summary of the basic ADPLL principle applicable to control systems and digital communication. It also reports components of ADPLL and comparison among them [3].

Nitesh Kumar et al (2013), told that the Operating frequency band of Radars vary depending on radar's emissions. This may lead to generate the necessity for selecting the spurious free band of operation. The spurious in a desired band of frequency can never be known a priori, rather than can be estimated only by practical experiments. The spurious in the frequency band is a critical parameter considering that it affects SFDR of radar received signal. Wide bandwidth waveform is required for finer resolution. His work describes the method of measuring in-band spurious masked under wide band LFM [4].

Govind S. Patel et al (2013), In this the authors introduced, an optimized Direct Digital Frequency Synthesizer (DDFS) utilizing Piecewise Linear Approximation. They proposed successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read later. The output of their proposed system is a reconstructed signal that is much closer to the desired waveform. As a result, the DDFS only needs to store fewer coefficients and the hardware complexity is significantly reduced. At the end, they concluded that the proposed DDFS has been analyzed using MATLAB and achieved 84.2 dBc. In future, it can also be used to improve the performance of Hybrid DDS-PLL Synthesizers [5].

M. NourEldin M. et al (2013), A low-power high-resolution ROM-less Direct Digital frequency synthesizer architecture based on FPGA Design is proposed. This work is equipped to generate a sinusoidal waveform with a new simple design method, which is endowed with high speed, low power, and high spurious-free dynamic range (SFDR) features. They had been proposed the low power methodology by two methods: first, in a phase accumulator design by selecting a pipelined phase accumulator with 8-bit components. And secondly the external powerless circuit of TSC. The output frequency of proposed design is 195.35 kHz using a built-in clock frequency of 50MHz. However, the maximum operating frequency is 190.93MHz. In addition, the design has the frequency resolution of 0.012Hz, which is promising to get very high tuning frequency with SFDR of 42 dBc or 70 dBFS [6].

III. DESIGN IMPLEMENTATION

Figure 1 shows the block diagram for the frequency synthesizer. The basic idea of this technique is the same with that used in above quadrant compression technique [3]. The first 2-bits are used to select the quadrants of the sine wave. The remaining N-2 bits are fed into Complement or whose output is split into two parts, the MSB part, with 3 bits long, represents the S segments and the LSB part with B bits long, represents an angle x in the interval $[0,\pi/(2S)]$. The segmented initial amplitudes Qi, represented with k bits are provided by a ROM. In our proposed block diagram the fetching and loading of successive coefficients are controlled by the pulse forming circuit. Besides the sine wave symmetry property, the linear approximation method has been used to approximate the first quadrant of sine function by S straight lines; each line is defined by two coefficients, Pi and Qi. The sine function in equation 1 is used for the calculation of approximated segment for the first quadrant of sine wave.

$$Pi = \{\sin [i\Delta x] - \sin [(i-1)\,\Delta x]\}/\,\Delta x \quad 1 \leq i \leq S \qquad (1)$$

Where, Δx = the length of segment. The Eq. 1 can easily be achieved by decreasing the Sin $[i\Delta x]$ at continuous phase angles and then again dividing the result by Δx. As Δx unsigned constant coefficient, the division can simply be obtained by normal binary operation. The coefficients, is equal to $[\sin (i-1)\,\Delta x]$ points, As examples for segment number1, (Q1= 0), yields K1 = P1x and for segment number 2, ($Q2 = \sin \Delta x$), in general, $Qi = \sin [(i-1)\,\Delta x]$ for the ith segment and it can be realized by delaying the pervious sin $(i\Delta x)$ by one clock period, hence the realization of the whole Ki (x) function is accomplished. Thus there are two consecutive sine points generated at a single time to start the processing of subtraction and extraction of the slope. These two sine points can be got only when the corresponding phase angles point simultaneously to their addresses in the sine LUT and that is an inconsequent assumption. As mentioned earlier, the accessing of the memory is valid only once at a specific clock cycle. In this study, we introduce architecture of pulse forming circuit which is performing the task of time sharing and propose the procedure enumerated below to get around this problem.

The Phase Accumulator, Phase-to-Amplitude Converter, Digital-to-Analog Converter and a Filter are the main components of a Digital Frequency Synthesizer. A frequency synthesizer is responsible for the generation of a sine wave at a specified frequency. The phase accumulator gets the input from the binary number in the phase register. The Phase accumulator is responsible to compute the phase angle. This phase angle is nothing but the address for a look-up table. The look-up table is a kind of a ROM which stores the digital value of amplitude. This amplitude value is equivalent to the phase angle for the sine wave. This value goes to the DAC, which converts that number into a corresponding of analog voltage or current. For the generation of fixed frequency sine wave, a constant value is added to the Phase Accumulator with each clock pulse. The phase increment is determined by the binary number M. In order to generate a high frequency sine wave the phase increment should be large. The large phase increment value forces the phase accumulator to step quickly to access the entire sine look-up table. In contrast, for small value of phase increment, the phase accumulator will take more steps and hence generates the slower waveform.

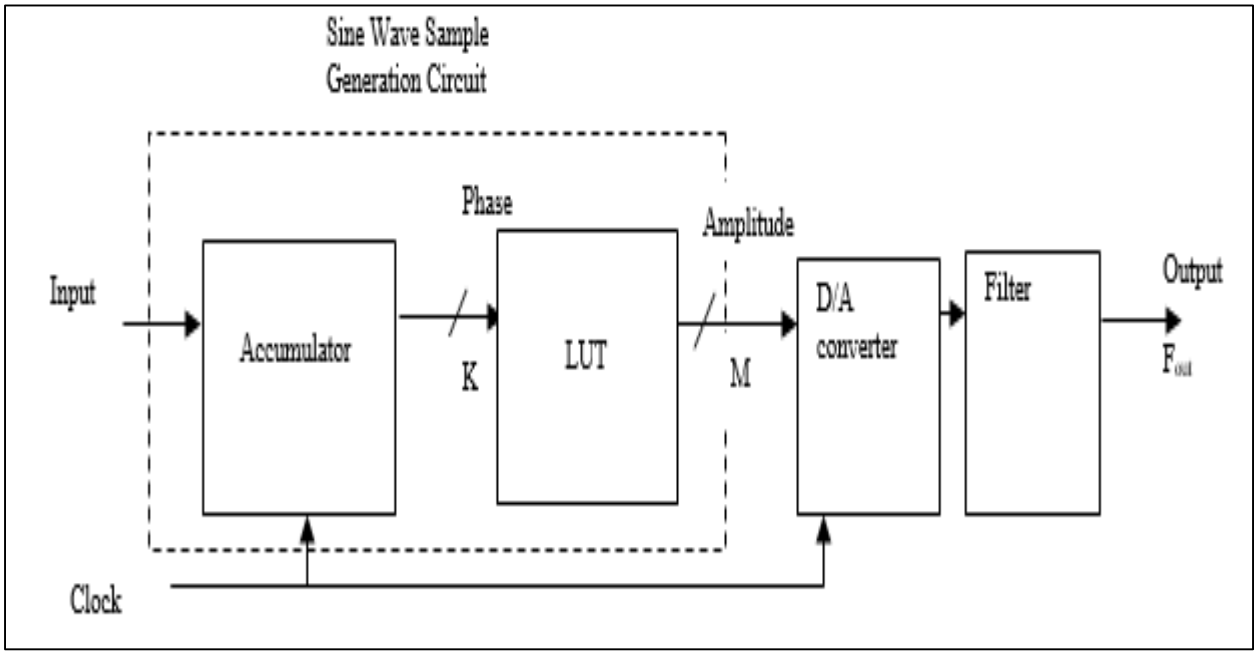

Fig. 1: Block diagram of a direct digital frequency synthesizer

A. Building Blocks of DDFS

As discussed above a frequency synthesizer has both the analog and digital blocks. The following section is gives the detail description of each and every block.

B. Phase Accumulator

The phase accumulator is contains a counter circuit which repeated itself after reaching its final value. As every real time signal always have an angular phase range of 0^o to 360^o, in a repetitive manner. Thus the digital implementation should also be repetitive in nature. Every time the counter reach its final value it is used to generate a carry signal which act as a phase wheel in the frequency synthesizer implementation.

C. Phase-to-Amplitude Converter (ROM/ LUT)

The frequency synthesizer's contains a sine Look-up Table work likes a ROM. This unit is responsible to convert the phase input to the output amplitude. The output from the accumulator represents the phase of the wave and an address of the corresponding amplitude of the phase in the sine Look-up Table. This amplitude value triggers the DAC to generate the analog signal.

D. Digital-to-Analog Converter and Filter

The phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude corresponding to the sine of that phase angle to the DAC. The DAC, in turn, converts that number to a corresponding value of analog signal typically Voltage or Current.

IV. RESULTS

This section shows the simulation results of the generated sine wave at 100 MHz clock frequency with different phase angles. Firstly we are providing the frequency-Tune-Word 21474830(d). One can also place this value in other digital format as per their convenience. The calculation of output frequency can be done by the formula:

Output_Freq = (FTW_in/2n)*Fsys. Where FTW_in is frequency Tune Word of N-bit length. And the Fsys is the system frequency i.e. 100 MHz (in our case).

The generation of sine wave at 0^o phase is shown in figure 2. For this, we provide only the Clk, and Pull down the Reset signal to 0.

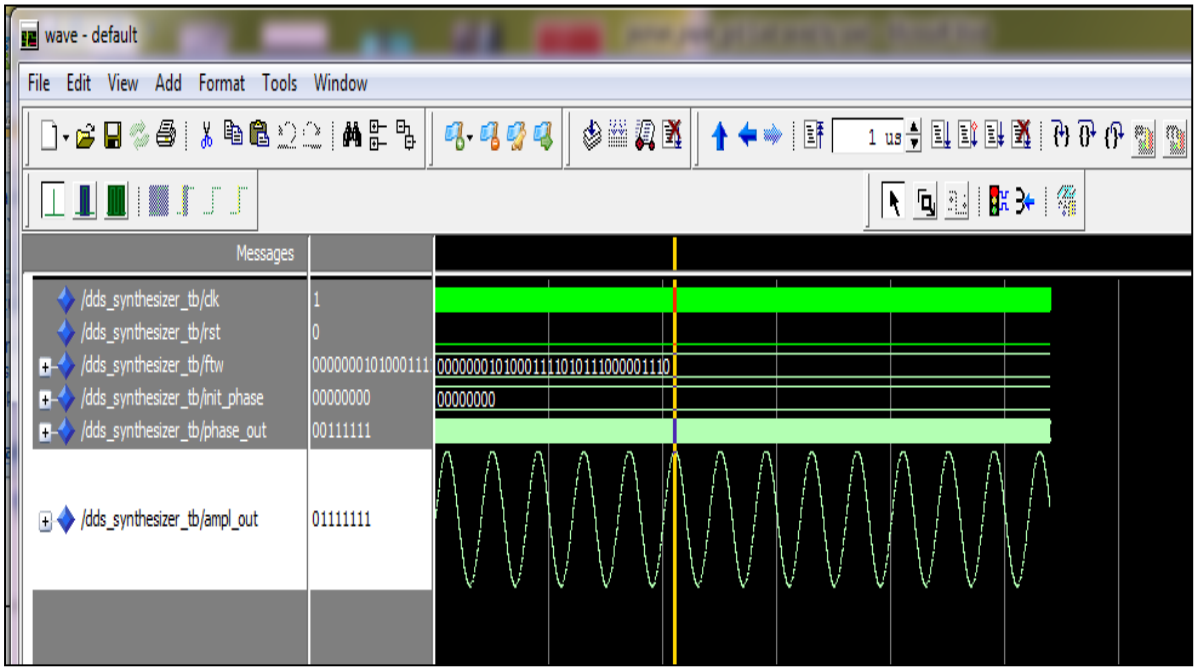

Fig. 2: Simulation result for 0º phase

Fig. 3: Simulation result for 90º phase shift

Figure 3 shows the output waveform for 90º phase shift of Sine wave. In this case we firstly change our phase angle value from degree to radian by the normal degree to radian conversion. And then convert the obtained value in the binary format. For this we had use the formula:

$1^o = (2\pi/360^o)$ radian

$90^o = (2\pi/360^o) * 90^o = \pi/2$ radian

For converting it into binary data => Radian value * 2^n

Here we used the 6-bits for converting the data while upper two bits for the quadrant, so Phase value for 90º is $(\pi/2) * 2^6$ i.e. approx. 100 in decimal and 64H in Hexadecimal.

Thus we can calculate the hex values for different Phase angle by the above method. Figure 4 & 5 shows the different waveform with some changes in the origin of the Sine wave. It is totally depends on the value of the phase angle we had provide.

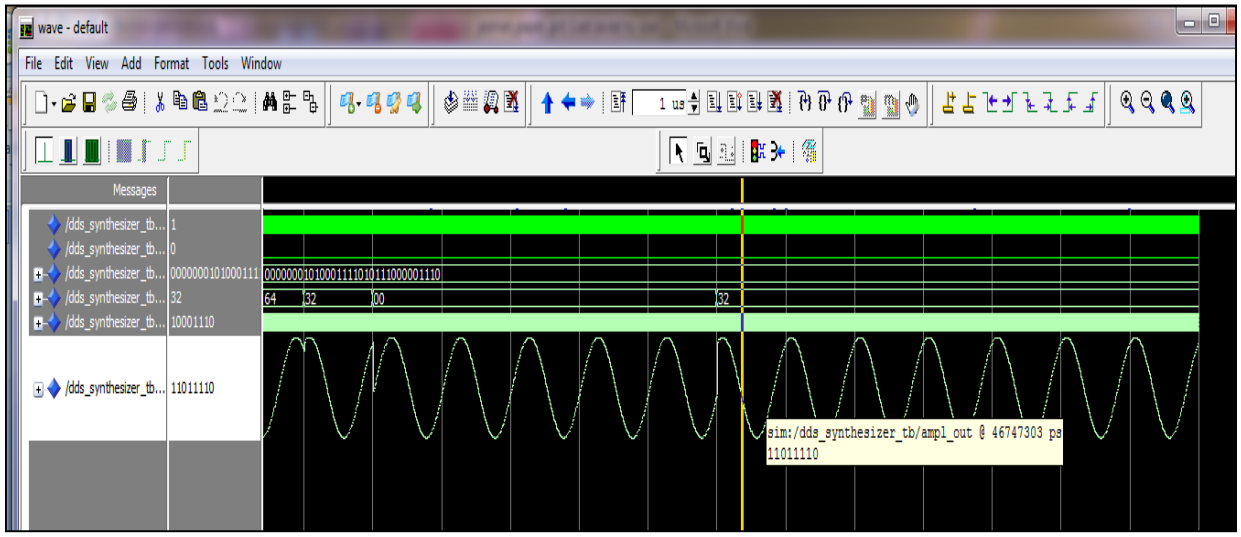

Fig. 4: Simulation result for 45º phase shift

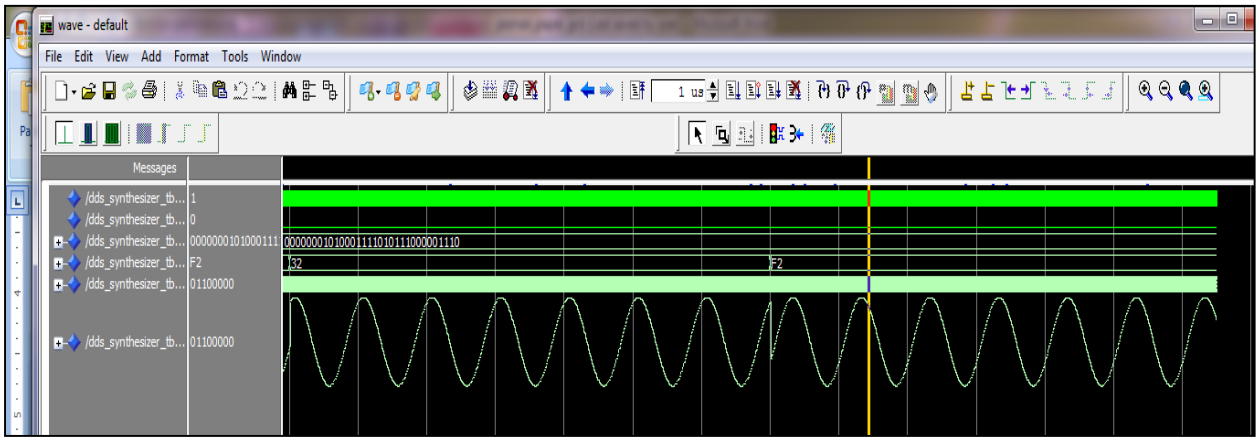

Fig. 5: Simulation result for -45º phase shift

Table 1: Device Utilization Summary

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	52	5472	0%
Number of Slice Flip Flops	64	10944	0%
Number of 4 input LUTs	100	10944	0%
Number of bonded IOBs	58	320	18%
Number of GCLKs	1	32	3%

V. CONCLUSION

The implementation of a direct digital frequency synthesizer (DDS) is also called number controlled oscillator (NCO). This produces a sine wave at the output with a 50 KHz frequency and phase (adjustable at runtime). The complete design has been synthesized and simulated with Xilinx ISE and Modelsim tool. The designer can increase or reduce the resolution of the frequency tuning word (FTW), the phase and the amplitude. The Sine_lut is generated by the using of MATLAB. Anyone can simulate this Digital Direct Frequency Synthesizer (DDFS) for Sine wave generation from 1Hz to 250 MHz with Amplitude -1V to 1V. To increase the speed of Sine wave generation is totally depends on the phase width. However the frequency range and amplitude level can be varied by changing the length of the tune word and amplitude output signal width.

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