A Review Paper on Memory Testing using BIST

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Abstract

In this review paper, Built-in self-test has been studied. This Built-in Self-Test (BIST) technique not only helpful from economically but also it gives test logic for the test pattern. This paper concluded basic test problems and some reliable methods of solution discussed in this paper while studied level of BIST. The basic concept of BIST that it provide a path by which system could test itself.

Keywords- Built-in Self-Test, Random Access Memory, CUT circuit under test, TPG Test Pattern Generation, Response Analysis, Pseudo-Random Test Generation, Fault Model

I. INTRODUCTION

Testing is a process of checking the fabricated chip against manufacturing defects, to determine the presence of a fault in a given circuit, no amount of test can guarantee that the circuit is fault free we carry out testing to validate the circuit. Two types of approaches are used to verify the circuit first is simulation-based approach and the second are the formal method [3]System board, chip, gate switch interconnection, logic function every part is tested. Adding some extra logic such that the memory can test itself whenever the test is enabled is called Design for Testing (DFT). There are some testing issues first one is testing at higher level cost higher, test application time grows exponentially e.g. For a combinational circuit with 60 input we need 2^60 test patterns are required, the third one is the lack of controllability and observability of flip-flops (test generation for sub sequential Circuit is difficult) basic test principal is input patterns are applied to the CUT and output is compared with the previously decided golden response to check whether it is good or not. [4]Memory is not composed of logic gates or flip-flops rather than these it is made up of a number of cells arranged in a symmetric manner As they have symmetry consumes less area than flip-flop or logic gates etc., Arranged in a compressed manner. Decrease in the memory price per bit due to quadrupled capacity every three years. High density implies decrease in size of capacitor used to store a bit (in experiments, it is found that if high dielectric capacity material is used in place of old ones like barium, tritium etc., Facility high capacitance maintained in less area) This memory cell only works to read and write these Cells as this cell comprises of 1 and 0 only. If we use flip-flop for memory building then we can observe it consumes more area with this it also not profitable in the market. Like general circuit, we do not discard faulty memory chips. Since every chip has defects so the faults are not only detected, but cell number is also diagnosed. [14] All memory cells will have a redundant circuit with them and it could be replaced by a faulty circuit. Capacitors are used to store bits if they charged they represent 1 if they are not they represents 0 values. Instead of the capacitor if flip-flops are used they lead to a very large area. The manufacturer builds some extra memory with the original one. Redundant circuit is switched by multiplexing arrangement or by blowing up with laser fuses.

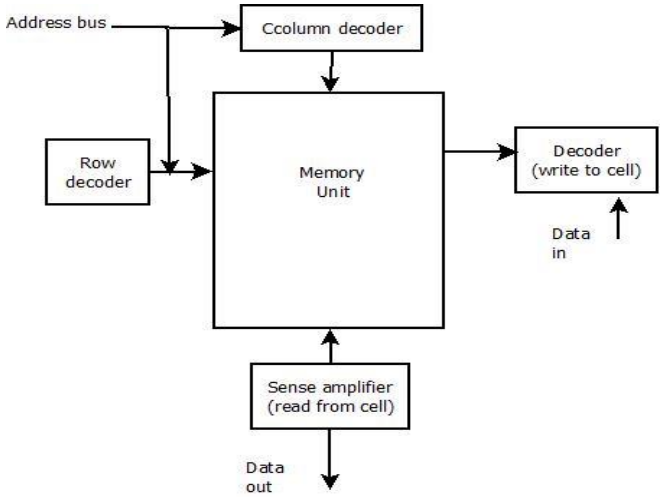

Fig. 1: Memory structure

A. Memory Cells

This is the unit which composed of a number of cells as they are arranged in a symmetric manner and it is a part where all RAM memory is present it holds value 1 and 0 in different cells, it has address bus and data bus in a parallel manner and they also have crossed arrangement of address and data bus, if address bus is active and it send 1 in data bus, the capacitor gets charged and shows 1 bit, and if in data bus we send 0 then its capacitor doesn't charge and shows 0, in this manner we can write data or read data in the memory. [1] [6]

B. Decoders

Two types of Decoders are found in the memory as the name implies they work for decoding data they are Row Decoder and column decoder.

The Row or Column Decoder are Implemented using logic gates, as they are digital circuits, they together collect information of row and column and fetch data from where it is to be accessed.

C. Sense Amplifier

This is an analog circuit, this amplifier used to sense whether to read data or not if it senses the command of read instruction it fetches the data, it has two units different to read and write.

D. Driver

The Driver is used to writing data on cells.

II. MEMORY TESTING AND FAULT TYPES

As we know memory is made up of the combination cells, arranged in a sequential manner these cells may be affected by many reasons such as they could have manufacturing faults, operational faults etc. These faults fail the system to perform an accurate operation. The memory unit has four major parts

1) A Read/write logic,
2) An Address decoder
3) A Sense amplifier
4) The Memory cell,

When any of this part is affected may cause failure, so it becomes essential to test and remove the fault. Among them, a few are explained here.

A. Stuck at Fault

A type of fault due to which cell does not change its state, it stuck at the previous state and become faulty, e.g. If any cell Stuck at zero, it does not change its value from 0 to 1 it remains at 0. It stays in its state and this cause failure, due to this it doesn't allow to fetch the accurate address or data value.

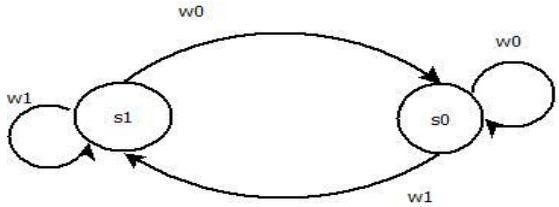

Fig. 2: At normal state

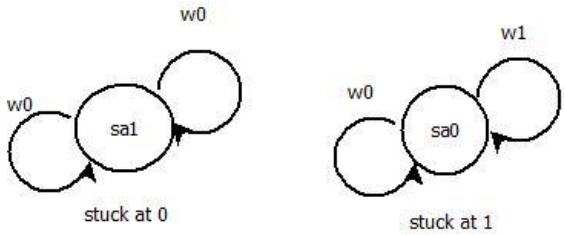

Fig. 3: Stuck at 0 and 1

B. Transition Faults

Transition fault is a special type of stuck at fault in which at write operation, it fails to write 1 and stay at its low state, hence it is called up transition fault, and if it unable to write 0 and stuck at 1 then this type of fat called us down transition fault. According to van de Goor [4] each cell must sustain an up transition (cell value goes from low to high) and a down transition (cell value goes from high to low) and be read after each transition before undergoing any further transition.

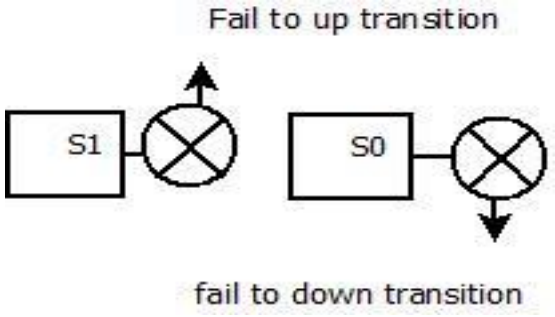

Fig. 4: Transition fault

C. Coupling Faults

Coupling faults are of three types [1].

1) Inverse coupling fault: due to some reason changes in the value of one cell unexpectedly inverts the content of another cell. [13]
2) Idempotent coupling fault: a change in one cell forces an affix logic value of one cell into another cell. [13]
3) State coupling fault: a cell is forced to a stay in its state only if the coupling cell/line is in a given state (pattern sensitivity fault (PSF)). [13]

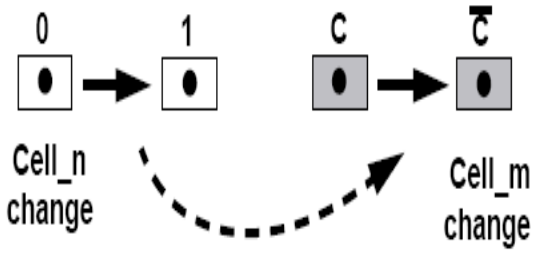

Fig. 5: Inversion coupling Fault Stuck-at Faults

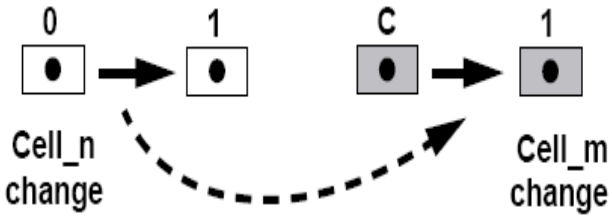

Fig. 6: Idempotent Coupling Fault

D. Bridging Fault

The Bridging fault is a type of fat which is determined by its logical level instead of transition write operation because it is caused due to the short circuit between two or more cells. We have found three types of bridging faults [13]

E. AND Bridging Fault

This is called so because the logical value of two faulty cells is AND of the two shortened cells acronym as ABF.

F. OR Bridging Fault

This is called so because the logical value of two faulty cells is OR of the two shortened cells acronym as OBF.

G. State Coupling fault

SCF is also a type of logical fault because a coupled cell is forced to certain value only because coupling cell is in that state.

H. Retention Faults (RF)

A cell fails to regain its logic value after some time. This fault is caused by a broken pull-up resistor.

I. Neighborhood Pattern Sensitive

The NPSF is a type of pattern sensitive fault in which cells are influenced by the neighboring cells; contents of cells are changed automatically by the transition of the neighboring cell from 0 to 1 or 1 to 0. Three types of NPSF faults are found: Active, Passive, and Static.

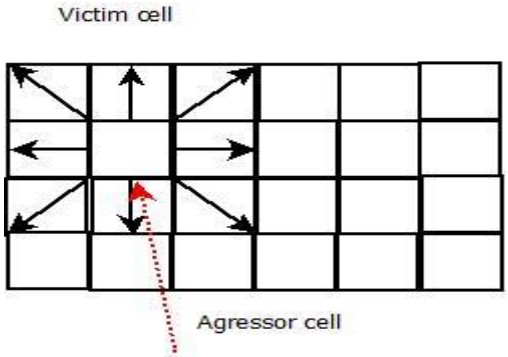

Fig. 7: Neighborhood Pattern Sensitive fault

J. Address Decoder Faults

During the read-write operation (AFs) address decoder faults are the fault due to which decoders are not able to fetch accurate address to fetch data, to simplify such problems we consider a different system in which each cell are tested is called bit oriented memory. The Functional fault within the address decoder can be classified into four AFs

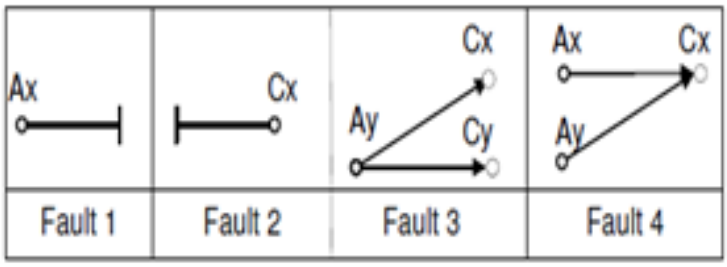

Fig. 8: Address decoder fault

For bit-oriented memories, because each cell is linked to a dedicated address, none of the faults listed above is individual. For example, when fault 1 occurs, then either fault 2 or fault 3 will occur as well. [4]

K. Linked Faults

Linked faults are more complex fault than the other faults explained in this paper in this type of faults many faults are linked with each other i.e. one fault occurs due to another one.

L. Data Retention Fault

Memory loses its content spontaneously not caused by read-write.

M. Recovery Fault

When some part of memory may not recover fast enough from its previous state, Sense amplifier recovery: after reading, writing long string of 0s and 1s, write recovery: write followed by read or write in a different location resulting in reading or writing at the same location.

N. Disturb Fault

Victim cell forced to 0 or 1 if we write aggressor cell.

III. FAULT MODELING

A circuit could have a number of physical defects in the circuit, it is not possible to consider individual so it is difficult to analyze each fault. As we can't test the whole circuit there is a limit to test faults. We cannot apply 2 ^n numbers of a test pattern, hence, fault modeling identifies the target fault and limits the scope of the test generation, make analysis possible, provide automatic and also manual test generation, fault simulation access the completeness of test models the fault at different approaches behavioral, functional, and structural. [7]

IV. BUILT IN SELF-TEST

As the technology is shrinking tested every part of the circuit is not affordable and challenges of testing are increasing exponentially, we need to use such circuit which can accurately test submicron part of the circuit and validate whether they are fault free or not, so BIST is a circuit which is designed to test faults before start up and provide a fault free circuit due to this it extend the lifetime of the electronic device. [7]

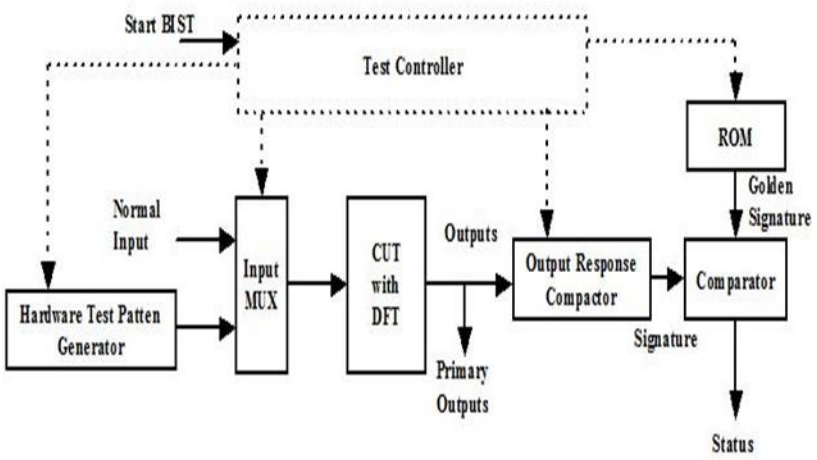

Fig. 9: Built In Self-Test Architecture

BIST test the CUT (in this project memory unit) generates test patterns for test and compare the output with golden response to the comparator output are already present in compressed form in ROM, by this circuit is tested and if any fault is found, it replaces the faulty part with appropriate part and provide a good circuit with this it also helps to repair memory

The Memory could have a number of defects already described in this paper could testing and also repaired through the BIST circuitry, many algorithms MARCHING, GALLOPING, MARCH TEST etc., Are developed, different type of fault needs different test patterns for them, In this proposed project we will design such circuit could be able to test a number of faults and repair them, the algorithm we design will consider three constraints of the testing area, power, and cost.

V. CONCLUSION

In this paper testing of memory and other modules has been studied using the built in self-test architecture. It has been seen that BIST architecture has ability to test on chip fault. This Built-in Self-Test (BIST) technique not only helpful from economically but also it gives test logic for test pattern. The simulation has been done by using VHDL/Verilog HDL Modalism and synthesize has been done by using the XILINX ISE Design Tool.

REFERENCES

[1] Nptel.ac.in/courses/106103016/30
[2] M. Abramovici, M. Breuer and A. Friedman, Digital Systems Testing and Testable Design, Piscataway, New Jersey: IEEE Press, 1994.
[3] E. McCluskey, "Built-In Self-Test Techniques," IEEE Design & Test of Computers, Vol. 2, No. 2, pp. 21-28, March 1985.
[4] R. A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," Hewlett-Packard Journal, vol. 28, no. 9, pp.
[5] Shaik Kari mullah G1, Abdul Rahim b C. Ushasree2." Design and verification of online BIST for Different word sizes of memories."
[6] Mrs. S. Enamel M.E1, T.Saranya2" Transparent Test Scheme in Online BIST for Word-Oriented Memories" ISSN 2278 – 0882
[7] M.H. Husin, S.Y. Leong, M.F.M. Sabri, R. Nordiana "Built in self test for RAM Using VHDL" 2012 IEEE Colloquium on Humanities, Science & Engineering Research (CHUSER 2012), December 3-4, 2012,
[8] Andreas Steininger" Testing and Built-in Self-Test" Institute für Technische Informatics, Vienna University of Technology A-1040 Vienna / Austria, Treitlstrasse 3
[9] V. Sridhar 1 M. Rajendra Prasad" Built-in self-repair (BISR) technique widely Used to repair embedded random access memories (RAMs)" International Journal of Computer Science Engineering (IJCSE)
[10] Version 2 IEEE IIT, Kharagpur" Built-In-Self-Test (BIST) for Embedded Systems"
[11] U. Siva Nagaraju, Dr. A. Sahaya Anselin Nisha Diagnosis and Fault Tolerance for Embedded BIST RAM International Journal of Scientific Research, Vol. III, and Issue. IV Apr 2014
[12] Sony Rama, Kishore Kumar and P. Rajesh Kumar. Sony integrated circuits and systems, vol. 30, no. 11, November Comp. SCI. & Engg. Elixir ISSN: 2229 -712x 41 (2011) 5579
[13] Chih-Sheng Hou, Jin-Fu Li, Member, IEEE, and Tsu-Wei Tseng IEEE transactions on computer-aided design of
[14] Sharvani Yedulapuram , Chakradhar Adupa International Journal of Computer Trends and Technology- volume2Issue1- 2011 ISSN:2231-2803 http://www.internationaljournalssrg.org Page 98 Online Testing of Word-oriented RAMs